GREEN Rectifier™ Controller Device

Check for Samples: UCC24610

FEATURES

- **Secondary-Side Controller Optimized for 5-V Systems**
- **Up to 600-kHz Operating Frequency**
- **V_{DS} MOSFET-Sensing**
- **1.6-Ω Sink, 2.0-Ω Source Gate-Drive Impedances**
- **Micro-Power Sleep Current for 90+ Designs**
- **Automatic Light-Load Management**
- **Synchronous Wake-Up From Sleep and Light-Load Modes**
- **Protection Features on Programming Inputs**
- **SYNC Input for CCM Operation**
- **20-ns Typical Turn-Off Propagation Delay**
- **Improved Efficiency and Design Flexibility Over Traditional Diode Solution**
- **May Be Biased Directly From 5-V Output**
- **Minimal Component Count**

APPLICATIONS

- **AC/DC 5-V Adapters**
- **5-V Bias Supplies**
- **Low Voltage Rectification Circuits**
- **Flyback and LLC Converters**

DESCRIPTION

This GREEN Rectifier™ controller is a high-performance controller and driver for standard and logic-level N-channel MOSFET power devices used for low-voltage secondary-side synchronous rectification.

The combination of controller and MOSFET emulates a near-ideal diode rectifier. This solution not only directly reduces power dissipation of the rectifier but also indirectly reduces primary-side losses as well, due to compounding of efficiency gains.

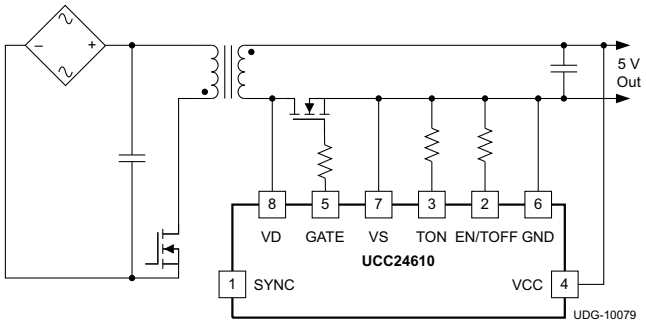
Using drain-to-source voltage sensing, the UCC24610 is ideal for Flyback and LLC-resonant power supplies but can also be used with other power architectures. The UCC24610 is optimized for output voltages from 4.5 V to 5.5 V, and is suitable for use with lower and higher output voltages as well.

The UCC24610 offers a programmable false-triggering filter, a programmable timer to automatically switch to Light-Load Mode at light load, and a SYNC input for optional use in Continuous Conduction Mode (CCM) systems. Protection features on TON and EN/TOFF pins prevent run-away on-time due to open-circuit or short-circuit fault conditions.

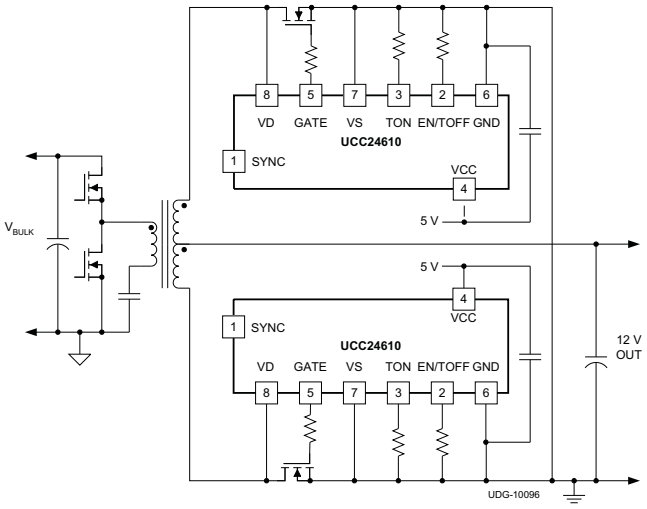
This device is available in an 8-pin SOIC package and an 8-pin, 3-mm x 3-mm QFN package with PowerPad™.

TYPICAL APPLICATIONS

Flyback Topology



LLC-Resonant Half Bridge



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PRODUCT INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE, T_A
UCC24610D	SOIC 8-Pin (D) Lead(Pb)-Free/Green	-40°C to 125°C
UCC24610DRB	QFN 8-Pin (DRB) Lead(Pb)-Free/Green	

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage range(2)	VCC	-0.3	6.5	V
	EN/TOFF(3)	-0.3	VCC	
	TON(4)	-0.3	VCC	
	VD for I_{VD} ≤ -10 mA	-1.0	50	
	VS for I_{VS} ≤ -10 mA	-1.0	0.5	
Input current, peak	SYNC(5) pulsed, t_{PULSE} ≤ 4 ms, Duty cycle ≤ 1%		±100	mA
Output current, peak	GATE(6) pulsed, t_{PULSE} ≤ 4 ms, Duty cycle ≤ 1%		±3	A
Human body model	HBM		2,000	V
Charged device model	CDM		500	
Junction temperature, T_J	Operating	-40	125	°C
	Storage	-65	150	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those included under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods of time may affect device reliability.

(2) Input voltages more negative than indicated may exist on any listed pin without excess stress or damage to the device if the pin’s input current magnitude is limited to less than -10mA. See separate ratings for SYNC and GATE pins.

(3) EN/TOFF can be driven by a voltage within the specified absolute maximum range or connected to a resistor to ground. Either method will program maximum off-time. When programmed by a resistor to GND, the voltage at the EN/TOFF terminal is internally limited to <VCC regardless of resistor value, so no absolute maximum input voltage considerations are required.

(4) In normal use, TON is connected to a resistor to GND. TON is normally not connected to a voltage source. When TON is connected to ground through a resistor, no absolute maximum input voltage considerations are required.

(5) In normal use, SYNC is connected with a capacitor to a high-speed voltage-transition source. The capacitor value shall be selected in conjunction with the worst-case voltage slew-rate to insure that the current into or out of SYNC is not in excess of the SYNC absolute maximum input current rating, or a current-limiting series resistor may also be necessary. In this use, if the input current is limited to less than the absolute maximum, no absolute maximum input voltage considerations are required. The capacitor breakdown voltage shall be selected to insure that dangerous voltage is not applied to the UCC24610. Continuous SYNC current is subject to the maximum operating junction temperature limitation.

(6) In normal use, GATE is connected to the gate of a power MOSFET through a small resistor. When used this way, GATE current is limited by the UCC24610 and no absolute maximum output current considerations are required. The series resistor shall be selected to minimize overshoot and ringing due to series inductance of the GATE output and power-MOSFET gate-drive loop. Continuous GATE current is subject to the maximum operating junction temperature limitation.

THERMAL INFORMATION

THERMAL METRIC[1]		UCC24610		UNITS
		D	DRB	
		8 PINS	8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance[2]	147	67	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	89	84.6	
θ_{JB}	Junction-to-board thermal resistance[4]	82	20.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[5]		7.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

All voltages are with respect to GND; currents are positive into and negative out of the specified terminal. −40°C < T_J = T_A < 125°C. (unless otherwise noted)

	PARAMETER	MIN	NOM	MAX	UNIT
V_{IN}	VCC input voltage	4.5		5.5	V
	VCC bypass capacitor	0.1		-	µF
T_J	Junction temperature	-40		125	°C
f_S	Switching frequency	20		600	kHz
	TON-to-GND resistor	10		261	kΩ
	EN/TOFF-to-GND resistor	93		280	
	SYNC pulse width at V_{THSYNC}-0.1V	20		-	ns

ELECTRICAL CHARACTERISTICS

At VCC = 5 V_{DC}, C_{GATE} = 0 pF, R_{TON} = 200 kΩ, $R_{EN/TOFF}$ = 100 kΩ, −40°C < T_J = T_A < 125°C, all voltages are with respect to GND, and currents are positive into and negative out of the specified terminal, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Bias Supply						
ICC_{START}	VCC current, undervoltage	VCC = 4.05 V	-	70	100	µA
ICC_{STBY}	VCC current, disabled	VCC = 5.5 V, $R_{EN/TOFF}$ = 0 Ω	-	130	200	
ICC_{ON}	VCC current, enabled	VCC = 5.5 V, $R_{EN/TOFF}$ = 100 kΩ	1.40	2.15	2.80	mA
VEN_{ON}	EN/TOFF turn-on threshold, rising	EN/TOFF driven, ICC > 1 mA	1.31	1.40	1.49	V
VEN_{OFF}	EN/TOFF turn-off threshold, falling	EN/TOFF driven, ICC < 200 µA	0.74	0.80	0.86	
$I_{EN-START}$	EN/TOFF input current, disabled	EN/TOFF = 1.3 V, rising from zero	-21.5	-20.0	-18.5	µA
I_{EN-ON}	EN/TOFF input current, enabled	EN/TOFF = 2 V	-10.7	-10.0	-9.3	
Under-Voltage Lockout (UVLO)						
VCC_{ON}	VCC turn-on threshold	Turn-on detected by V_{EN} > 1.0 V	4.15	4.40	4.65	V
VCC_{OFF}	VCC turn-off threshold	Turn-off detected by V_{EN} < 0.5 V	3.96	4.20	4.44	
VCC_{HYST}	UVLO hysteresis	VCC_{HYST} = VCC_{ON} - VCC_{OFF}	0.15	0.20	0.25	
MOSFET Voltage Sensing						
V_{THARM}	GATE re-arming threshold	VD to GND, rising	1.3	1.5	1.7	V
V_{THON}	GATE turn-on threshold	(VD – VS) falling, VS = 0 V	-220	-150	-80	mV
V_{THOFF}	GATE turn-off threshold	(VD – VS) rising, VS = 0 V	-8	-5	-2	
t_{DON}	GATE turn-on propagation delay	From V_{THON} to GATE > 1 V	-	44	70	ns
t_{DOFF}	GATE turn-off propagation delay	From V_{THOFF} to GATE < 4 V	-	16	35	
I_{DH}	VD input bias current, high	VD = 50 V, VS = 0 V	-	0.05	2.00	µA
I_{DL}	VD input bias current, low	VD = -0.15 V, VS = 0 V	-250	-150	-50	
I_S	VS input bias current	VD = 0 V, VS = 0 V	-250	-150	-50	
Minimum On-Time Setting						
T_{ONLR}	Minimum on-time, low resistance	R_{TON} = 16.5 kΩ	0.17	0.25	0.33	µs
T_{ONHR}	Minimum on-time, high resistance	R_{TON} = 200 kΩ	2.2	3.0	3.8	

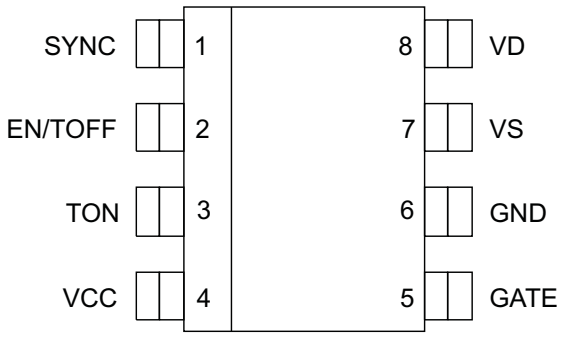
ELECTRICAL CHARACTERISTICS (continued)

At VCC = 5 V_{DC}, C_{GATE} = 0 pF, R_{TON} = 200 kΩ, $R_{EN/TOFF}$ = 100 kΩ, −40°C < T_J = T_A < 125°C, all voltages are with respect to GND, and currents are positive into and negative out of the specified terminal, unless otherwise noted. Typical values are at T_J = 25°C.

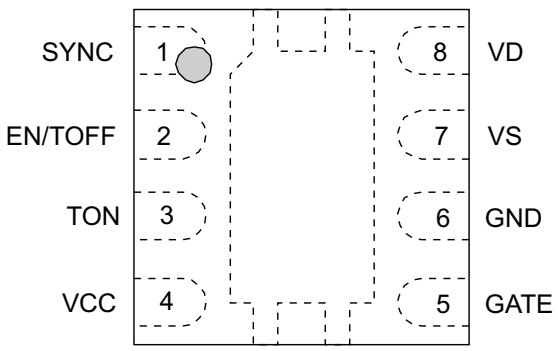
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Off-Time Setting						
T_{OFFLR}	Minimum off-time, low resistance	$R_{EN/TOFF}$ = 100 kΩ	4.94	7.80	9.86	µs
T_{OFFHR}	Minimum off-time, high resistance	$R_{EN/TOFF}$ = 261 kΩ	0.55	1.37	2.30	
T_{OFFLV}	Minimum off-time, low voltage	EN/TOFF = 1.0 V	4.94	7.80	9.86	
T_{OFFHV}	Minimum off-time, high voltage	EN/TOFF = 2.61 V	0.85	1.37	2.10	
T_{OFFOV}	Minimum off-time, over-voltage	3 V < V_{EN} < VCC	0.48	0.65	0.82	
Gate Driver						
r_{GUP}	GATE pull-up resistance, enabled	I_{GATE} = -100 mA	-	2.0	3.6	Ω
r_{GDN}	GATE pull-down resistance, enabled	I_{GATE} = 100 mA	-	1.6	2.5	
V_{OHG}	GATE output high voltage	I_{GATE} = -100 mA	4.64	4.80	-	V
V_{OLG}	GATE output low voltage	I_{GATE} = 100 mA	-	0.16	0.25	
V_{OLGUV}	GATE output low voltage, UV	I_{GATE} = 25 mA, VCC = 0 V	-	0.70	0.90	
V_{OLGOFF}	GATE output low voltage, disabled	I_{GATE} = 25 mA, V_{EN} = 0 V	-	0.04	0.10	
t_{fGATE}	GATE rise time	From 1 V to 4 V, C_{GATE} = 3300 pF	-	14	30	ns
t_{rGATE}	GATE fall time	From 4 V to 1 V, C_{GATE} = 3300 pF	-	9	25	
t_{DIS}	Disable delay	From EN falling to GATE falling	50	100	150	
Synchronization						
V_{THSYNC}	SYNC falling threshold	GATE output transitions from High to Low.	VCC - 2.4	VCC - 2.0	VCC - 1.6	V
t_{SDLY}	SYNC propagation delay	From SYNC falling to GATE falling 10%.	-	20	60	ns
r_{SYNC}	SYNC pull-up resistance	Internal resistance from SYNC to VCC.	1.6	2.0	2.4	kΩ

DEVICE INFORMATION

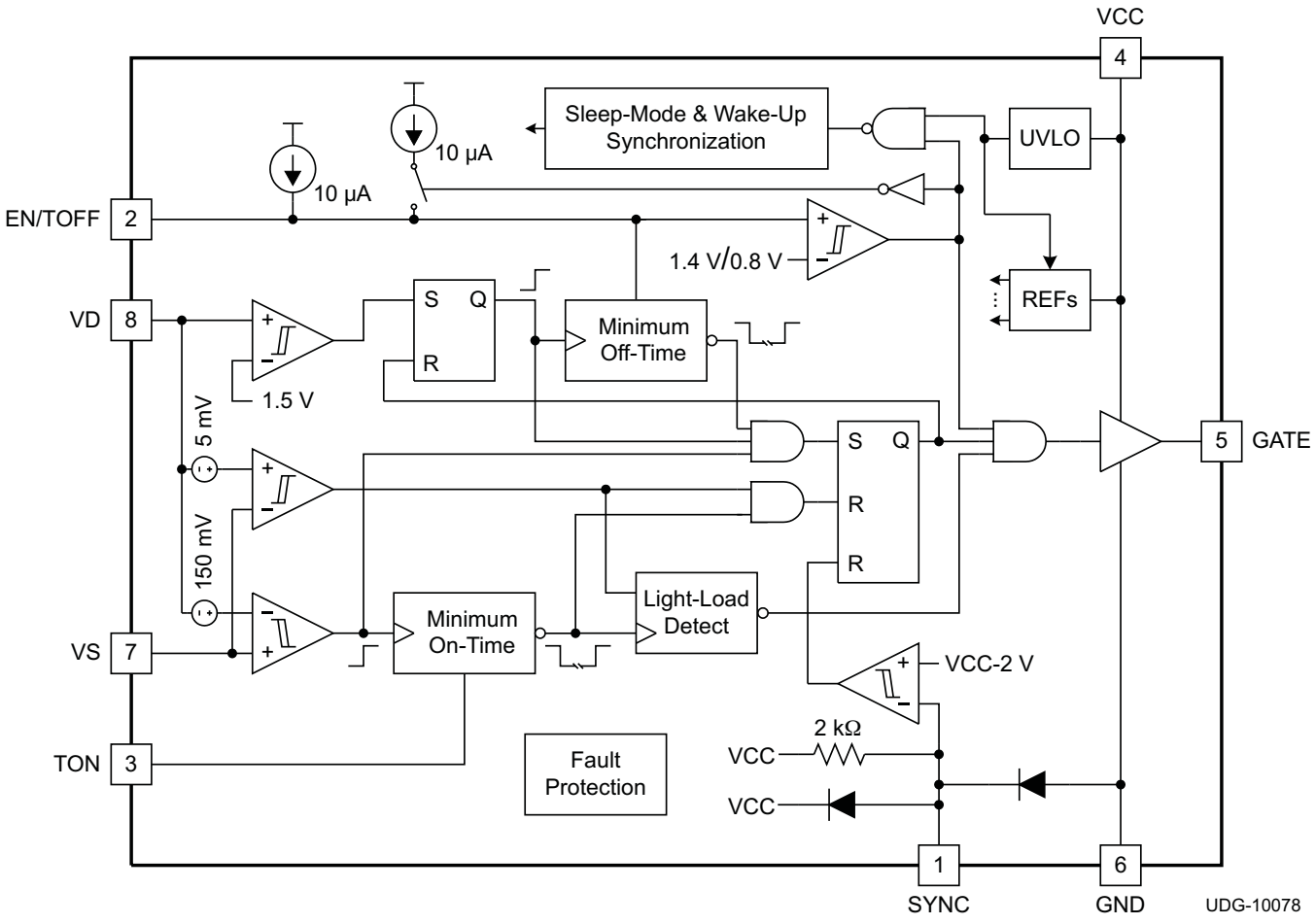
SOIC 8-Pin (D)



QFN-8 (DRB)



Functional Block Diagram



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EN/TOFF	2	I	**EN/TOFF (Combined Enable Function & Programmable Off-Time Timer)** When VCC falls below the $V_{CC(off)}$ threshold, the UCC24610 is in UVLO Mode, the EN/TOFF input is internally connected to GND through a 10-kΩ resistance and the internal current source is turned off. When VCC exceeds the $V_{CC(on)}$ threshold, the 10-kΩ resistance is removed and the current source is turned on. Thereafter, when EN/TOFF exceeds $V_{EN(on)}$, the UCC24610 is in Run Mode and when EN/TOFF falls below $V_{EN(off)}$, the UCC24610 is in Sleep Mode. The voltage level on EN/TOFF also programs the minimum off-time (T_{OFF}) for the controlled MOSFET. EN/TOFF is internally driven by a two-level current source, so the voltage level on EN/TOFF can be set by connecting a resistor from EN/TOFF to GND. The EN/TOFF current source initially drives twice as much current ($I_{EN-START}$) to achieve the enable threshold voltage $V_{EN(on)}$, and then drops to the normal Run Mode level (I_{EN-ON}) to program the T_{OFF} time. Alternatively, the desired EN/TOFF voltage may be forced using an external source. The T_{OFF} time is programmed to suppress GATE output for a desired duration to avoid possible false retriggering from resonant ringing or noise after turn-off. The T_{OFF} timer is triggered when VD voltage exceeds 1.5 V after GATE transitions from high to low.
GATE	5	O	**GATE (Controlled MOSFET Gate Drive)** Connect GATE to the gate of the controlled MOSFET through a small series resistor using short PC board tracks to achieve optimal switching performance. The GATE output can achieve >1-A peak source current when High and >2-A peak sink current when Low into a large N-channel power MOSFET. In Sleep Mode and UVLO, GATE impedance to GND is about 1.6 Ω. GATE impedance to GND crests about 80 Ω, when VCC ≈ 1.1 V.
GND	6		**GND (Combined Analog and Power Ground)** This ground input is the reference potential for the GATE driver, the UVLO comparator, the EN/TOFF comparator, the EN/TOFF timer, and the TON timer. Connect a 0.1-µF or larger ceramic bypass capacitor from the VCC pin to the GND pin through very short PC-board tracks.
PowerPad™	9		**PowerPad™ (Thermal Pad on QFN package only)** The exposed pad (PowerPad™) on the bottom of the QFN package enhances the thermal performance of the device, and is intended to be soldered to a heat-dissipating pad on the PCB. This pad should be connected to the GND pin, or may be left floating (unconnected to any network). It is internally connected to GND through an indeterminate impedance and so may not be used to carry current.
SYNC	1	I	**SYNC (Gate Turn-Off Synchronization)** A falling edge on SYNC immediately forces GATE low, turning off the controlled MOSFET asynchronous to the voltage on the drain and source, and regardless of the state of the TON timer. When a power converter is operated in Continuous Conduction Mode (CCM), it is necessary to turn off the controlled MOSFET under command of the switching converter. Connect SYNC to a control signal on the primary side of the converter using a high-voltage isolation capacitor or transformer, or other suitable coupling means. A continuous low level on the SYNC input causes GATE to be driven low for the same duration.
TON	3	I	**TON (Programmable On-Time Timer)** Program the minimum on time with a resistor from TON to GND. When the controlled MOSFET gate is turned on, some ringing noise is generated. The minimum on-time timer blanks the VD-VS comparator, keeping the controlled MOSFET on for at least the programmed minimum time. This time also determines the light-load shut-down point. If VD-VS falls below the -5-mV threshold before TON time expires, the controller transitions into Light-Load Mode on the next switching cycle. When VD-VS falls below the -5-mV threshold after TON expires, the device resumes Run-Mode operation on the next switching cycle.

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VCC	4	I	**VCC (Positive Power Input)** Connect a DC power voltage to VCC. Bypass VCC to GND with a 0.1-µF or larger ceramic capacitor using short PC board tracks. VCC supplies power to all circuits in the UCC24610. Under-Voltage Lockout (UVLO) comparators prevent operation until VCC rises above $V_{CC(on)}$. VCC can be used to safely turn off the UCC24610 by pulling VCC below $V_{CC(off)}$. In the event that VCC drops below $V_{CC(off)}$, GATE immediately falls Low and EN/TOFF is internally connected to GND with a 10-kΩ resistance.
VD	8	I	**VD (Drain-Sense Voltage)** Connect this pin as close as possible to the controlled MOSFET drain pad through a short PC board track, to minimize the effects of trace inductance on VD. VD must be >1.5 V and the TOFF timer must be expired before the device may be armed to allow the controlled MOSFET to be turned on the next switching cycle. Once armed, the controlled MOSFET is turned on (GATE goes High) when VD falls more than -150 mV below VS. At that threshold, the GATE output goes High and the TON timer is triggered. GATE remains High at least as long as the programmed TON time has not expired, unless a pulse at the SYNC input is detected. After TON has expired, the GATE output is turned off when VD-VS voltage decreases to -5 mV. If VD-VS decreases to -5 mV before TON expires, the controller enters Light-Load Mode and the GATE pulse for the next switching cycle is suppressed. When the VD voltage increases to 1.5 V, the TOFF timer is triggered and the GATE output is prevented from turning on during the TOFF interval.
VS	7	I	**VS (Source-Sense Voltage)** Connect this pin as close as possible to the controlled MOSFET source pad through a short PC-board track, to minimize the effects of trace inductance on VS.

MODES OF OPERATION

UVLO Mode

When the VCC voltage to the device has not yet reached the $V_{CC(on)}$ threshold, or has fallen below the UVLO threshold $V_{CC(off)}$, the device operates in the low-power UVLO Mode. In this mode, most internal functions are disabled and ICC current is typically much less than 100 µA. While in this mode, the EN current source is shut off, an internal 10-kΩ resistance is applied from the EN/TOFF pin to GND, the voltage on EN/TOFF is irrelevant, and the GATE output is driven low continuously for all VCC > 1.2 V. The device passes out of UVLO Mode when VCC increases above the $V_{CC(on)}$ threshold. UVLO Mode is very similar to Sleep Mode, except VCC current is at $I_{CC(start)}$ level.

Sleep Mode

Sleep Mode is a low-power operating mode similar to UVLO Mode, except that this mode is entered under external control by forcing V_{EN} below the $V_{EN(off)}$ threshold. Sleep Mode may be used to reduce device operating losses to less than 1 mW. VCC current reduces to $I_{CC(stby)}$ level. External control overrides any internal timing conditions, and immediately forces the GATE output low and enters Sleep Mode. Many internal circuits are turned off to reduce power consumption. When V_{EN} is restored to above the $V_{EN(on)}$ threshold, the device exits Sleep Mode synchronously into Light-Load Mode after a delay of approximately 25 µs to allow re-powered internal circuits to settle.

Run Mode

Run Mode is the normal operating mode of the controller when not in UVLO Mode, Sleep Mode, or Light-Load Mode. In this mode, VCC current is higher because all internal control and timing functions are operating and the GATE output is driving the controlled MOSFET for synchronous rectification. VCC current is the sum of $I_{CC(on)}$ plus the average current necessary to drive the load on the GATE output. GATE output duty-cycle is dependent upon system line and load conditions, programmed TON and TOFF times, and SYNC-pulse timing (if applicable).

Light-Load Mode

Light-Load Mode is a low-power operating mode similar to Sleep Mode, except that this mode is entered automatically based on internal timing conditions. Light-Load Mode automatically reduces switching losses under light-load conditions by suppressing GATE output pulses whenever the detected synchronous conduction time is less than the programmed minimum on-time (TON). VCC current reduces to $I_{CC(on)}$ level. While in Light-Load Mode, the MOSFET body-diode conduction time is still continuously monitored. When this time is detected to once again exceed TON, the device resumes Run Mode on the next switching cycle.

Fault Mode and Other Protections

Fault Mode is a self-protection operating mode of the controller when certain types of single-fault conditions are detected on certain pins. In this mode, the device enters a shut-down state (not Sleep Mode) and drives the GATE output Low. Specifically, Fault Mode is entered if R_{TON} > 301 kΩ or if R_{TON} < 8.7 kΩ. Fault Mode prevents the conditions of excessive or indefinite on-time (such as from an open-pin) and of excessive TON current (such as from a shorted-pin).

Similar protection is provided for the EN/TOFF pin. While not specifically detected as faults, if this pin becomes open-circuited TOFF defaults to a minimum value of ~0.65 µs, and if shorted-to-GND the device enters Sleep Mode. Additionally, if the SYNC input is continuously held below its trigger threshold voltage, the GATE output is held low for the entire duration that SYNC remains in that condition.

TYPICAL CHARACTERISTICS

BIAS SUPPLY CURRENT vs BIAS SUPPLY VOLTAGE

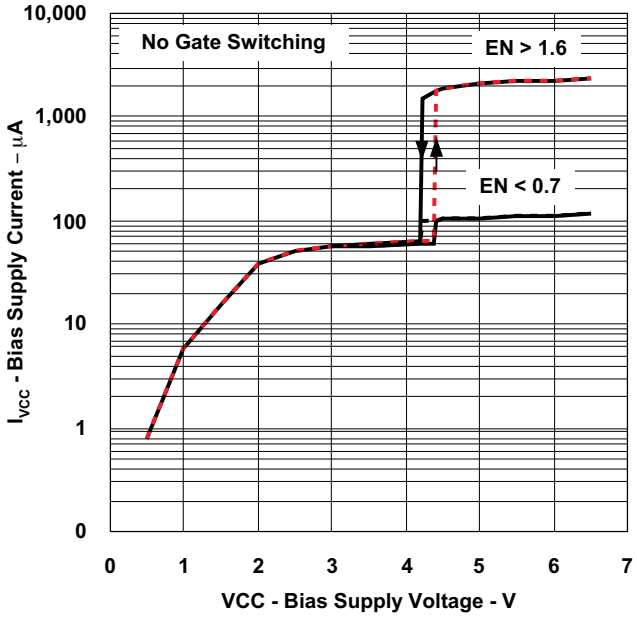


Figure 1.

THRESHOLD VOLTAGE vs TEMPERATURE

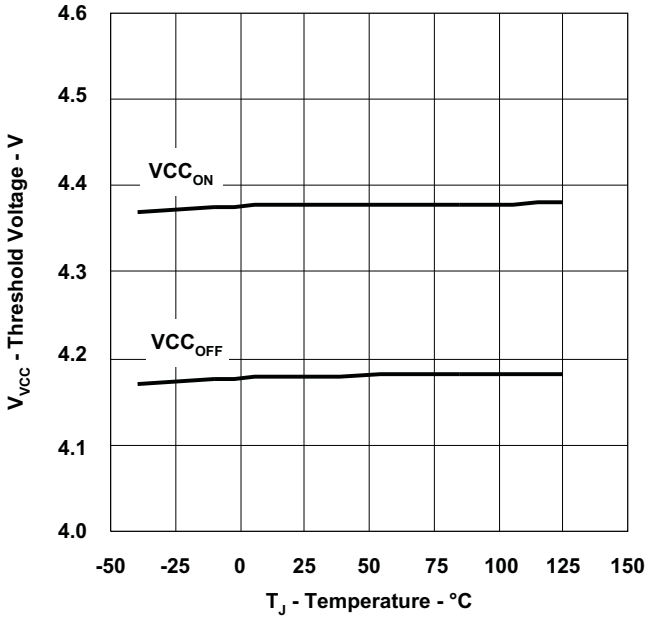


Figure 2.

BIAS SUPPLY CURRENT vs TEMPERATURE

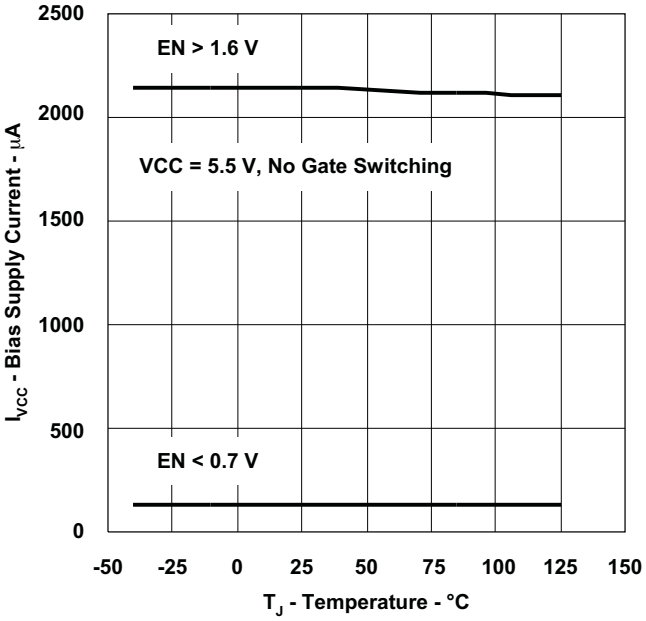


Figure 3.

SUPPLY CURRENT vs SWITCHING FREQUENCY

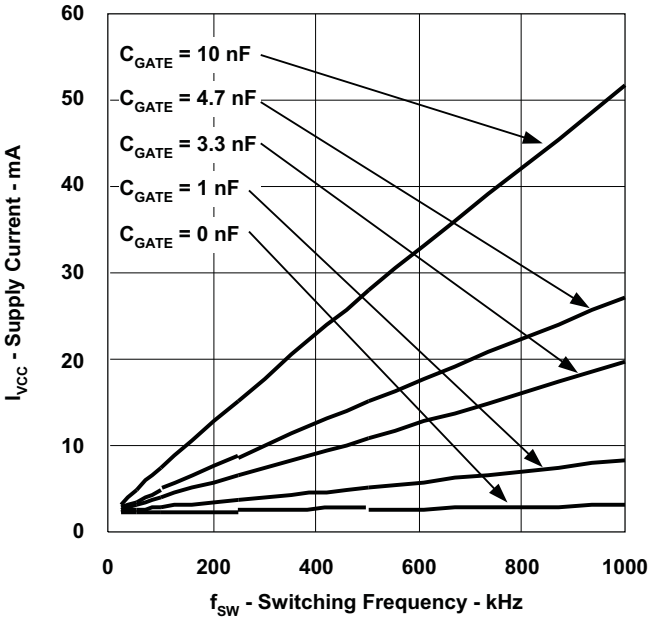


Figure 4.

TYPICAL CHARACTERISTICS (continued)

ENABLE CURRENT vs TEMPERATURE

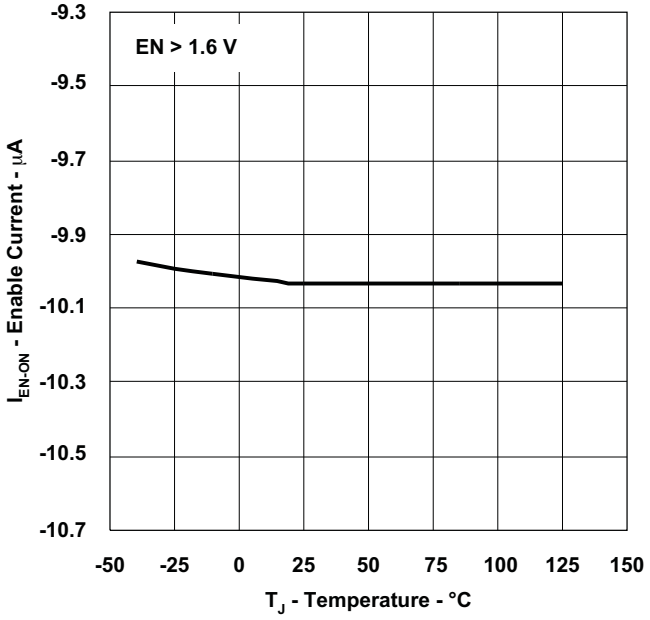


Figure 5.

THRESHOLD VOLTAGE vs TEMPERATURE

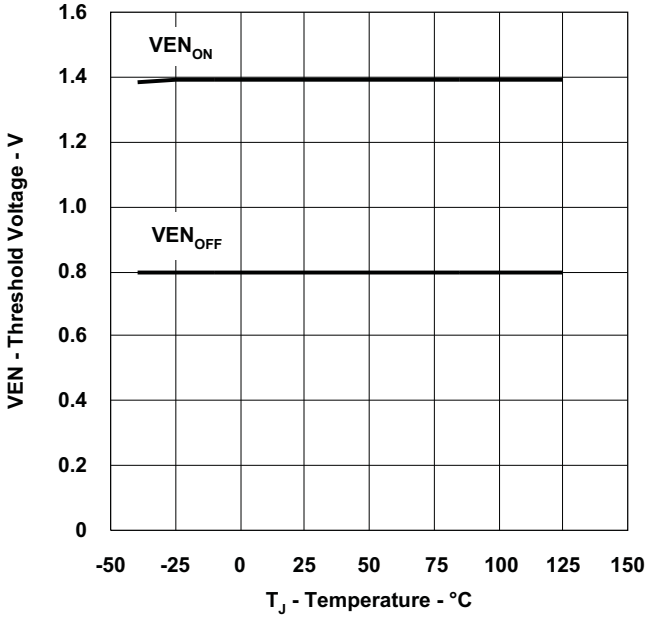


Figure 6.

SYNC THRESHOLD VOLTAGE vs TEMPERATURE

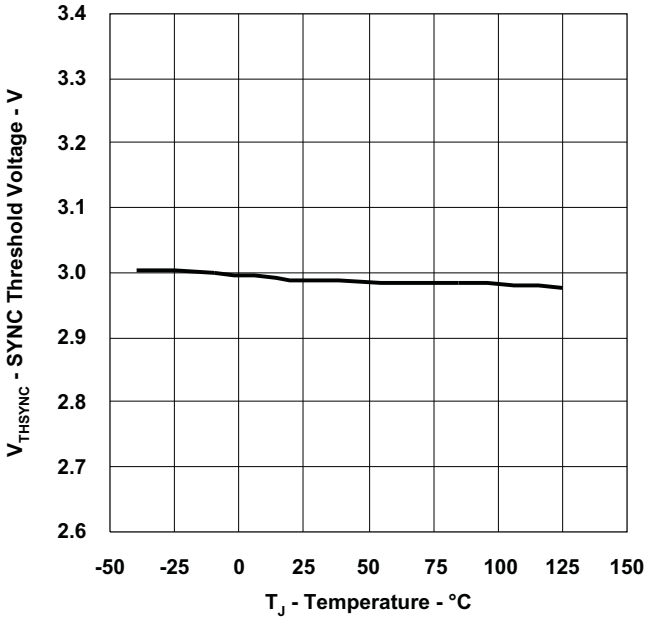


Figure 7.

SYNC PROPAGATION DELAY TIME vs TEMPERATURE

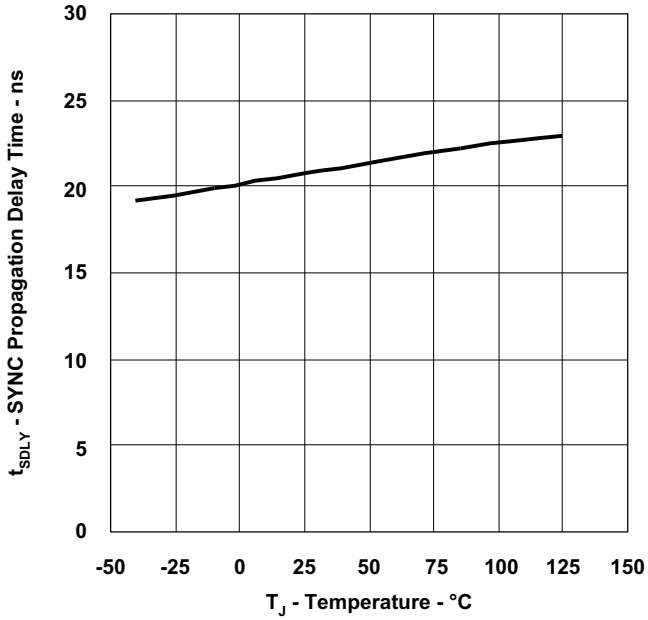


Figure 8.

TYPICAL CHARACTERISTICS (continued)

V_{DS} GATE-OFF THRESHOLD VOLTAGES vs TEMPERATURE

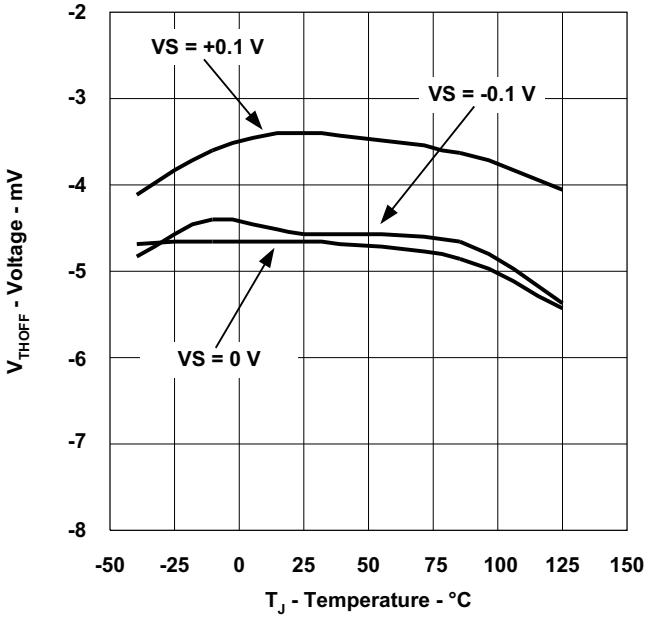


Figure 9.

V_{DS} GATE-ON THRESHOLD VOLTAGE vs TEMPERATURE

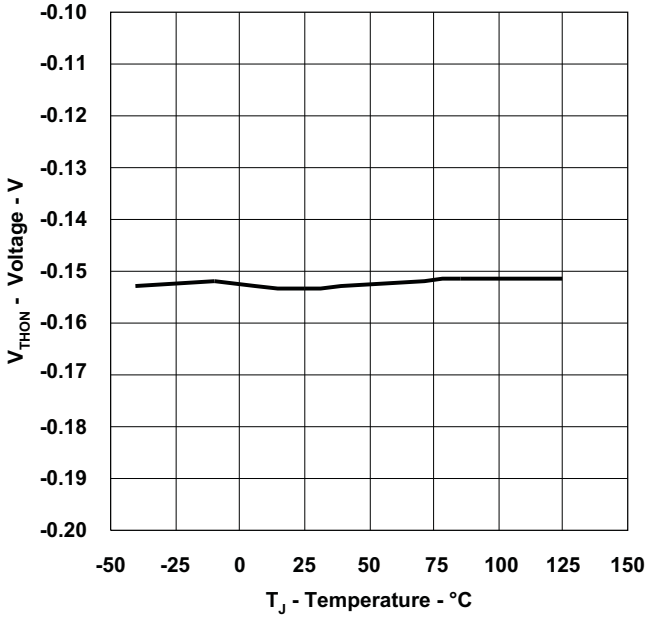


Figure 10.

GATE PROPAGATION DELAY TIME vs TEMPERATURE

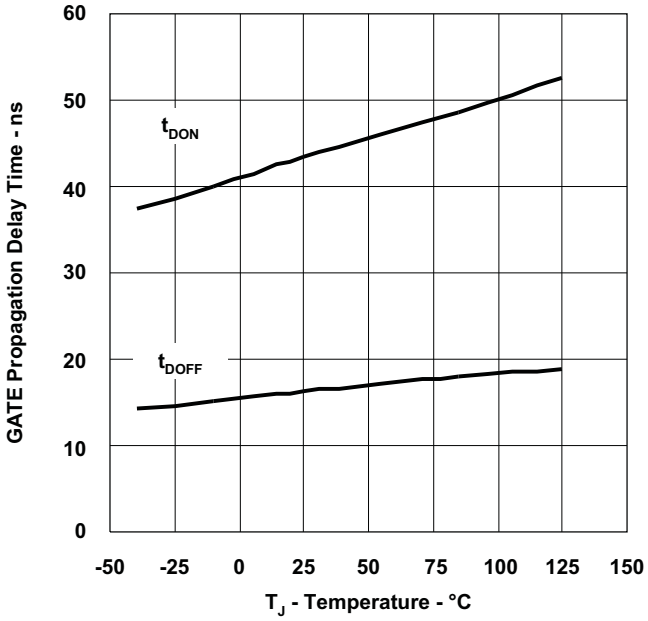


Figure 11.

GATE RISE AND FALL TIME vs TEMPERATURE

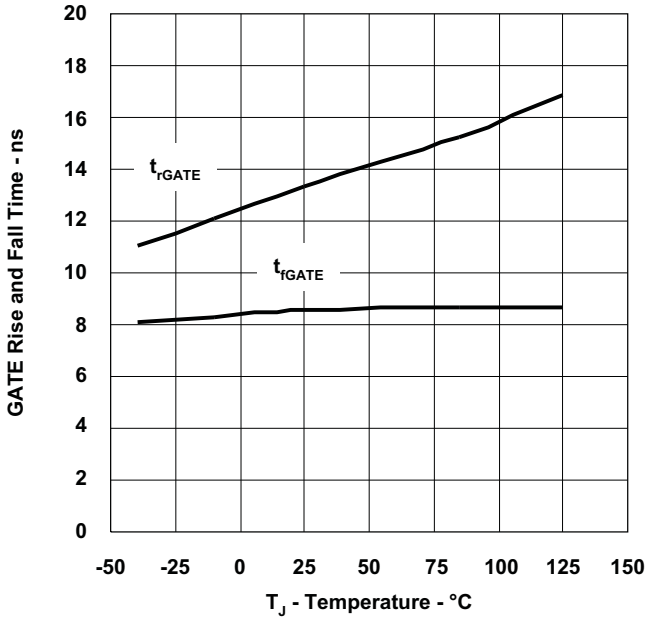


Figure 12.

TYPICAL CHARACTERISTICS (continued)

MINIMUM ON TIME vs TON RESISTANCE

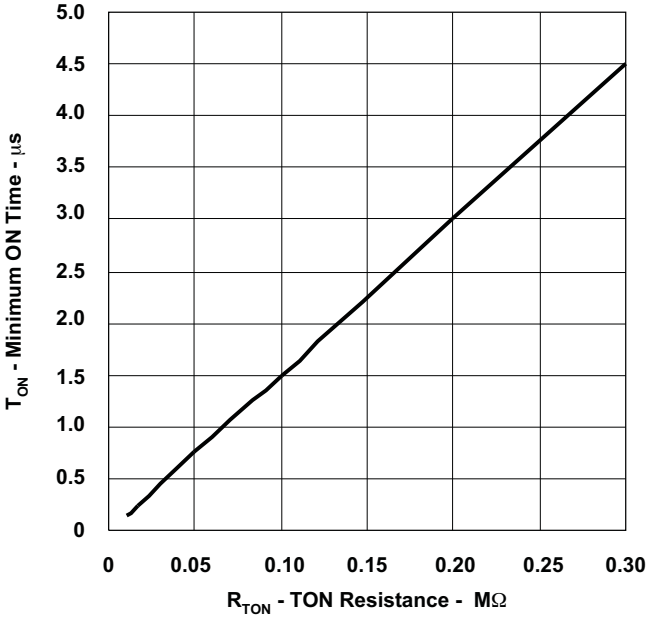


Figure 13.

MINIMUM OFF TIME vs TOFF RESISTANCE

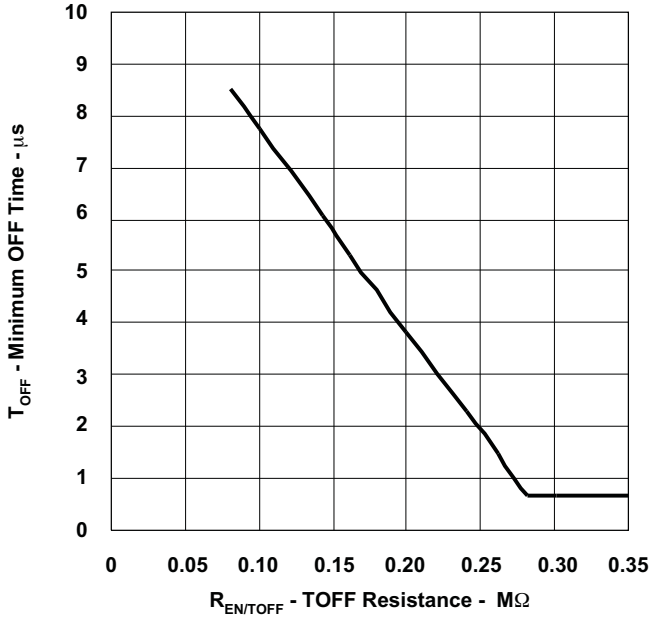


Figure 14.

T_{ON} AND T_{OFF} TIME vs TEMPERATURE

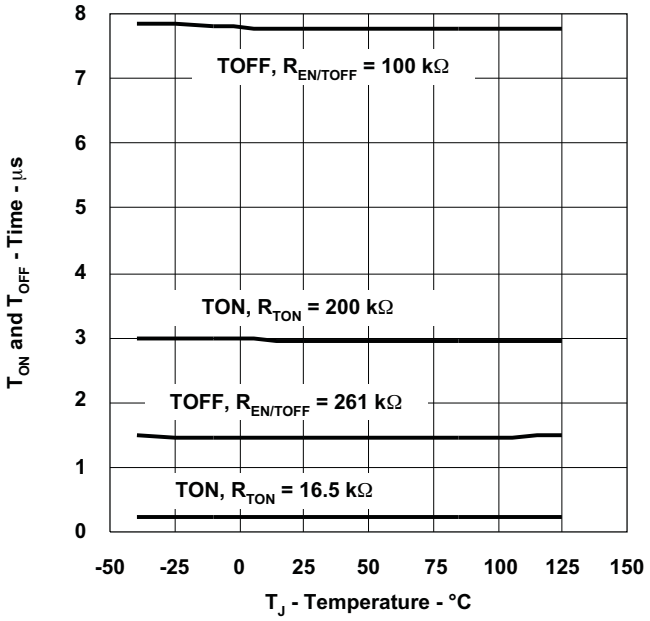


Figure 15.

VD BIAS CURRENT vs DRAIN SENSE VOLTAGE

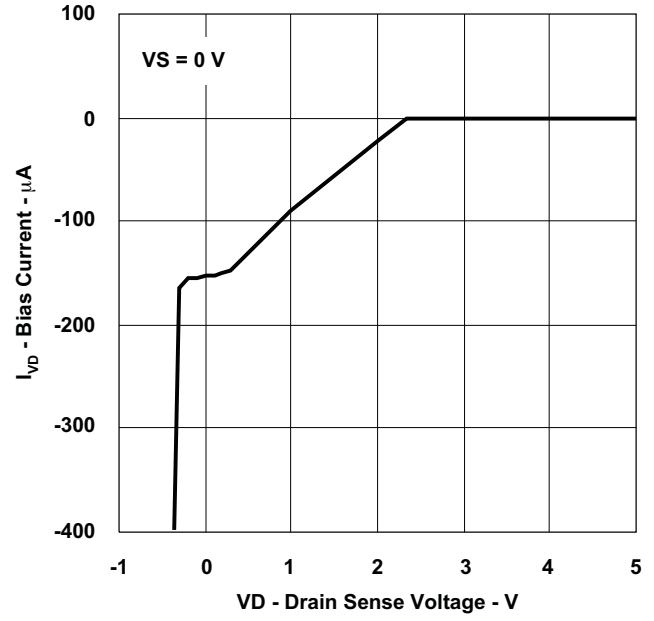


Figure 16.

APPLICATION INFORMATION

Normal Operation

The UCC24610 GREEN Rectifier™ Synchronous-Rectifier (SR) controller powers up into UVLO Mode as VCC increases from zero volts. Enable Current (I_{EN}) from the EN/TOFF pin is inhibited until VCC exceeds the $V_{CC(on)}$ threshold, and remains active as long as VCC exceeds the $V_{CC(off)}$ threshold. The voltage on the EN/TOFF pin determines whether the controller is Enabled or not. The controller operates in the normal Run Mode when the Enable Voltage (VEN) exceeds the Enable threshold $V_{EN(on)}$ and remains enabled as long as V_{EN} exceeds the $V_{EN(off)}$ threshold.

After the controller is Enabled, V_{EN} programs the minimum off time inversely proportional to the voltage (see T_{OFF} section). The two-state Enable current allows a lower-value resistance for $R_{EN(off)}$ (necessary to program longer off time) to still generate sufficient voltage to exceed $V_{EN(on)}$ at start-up. A simple resistor from EN/TOFF to GND generates V_{EN} based on the level of I_{EN} current flowing through it. See Figure 17. Alternatively, V_{EN} may be driven by an external voltage source provided this voltage exceeds $V_{EN(on)}$ for at least 100 ns before settling to its final programming level.

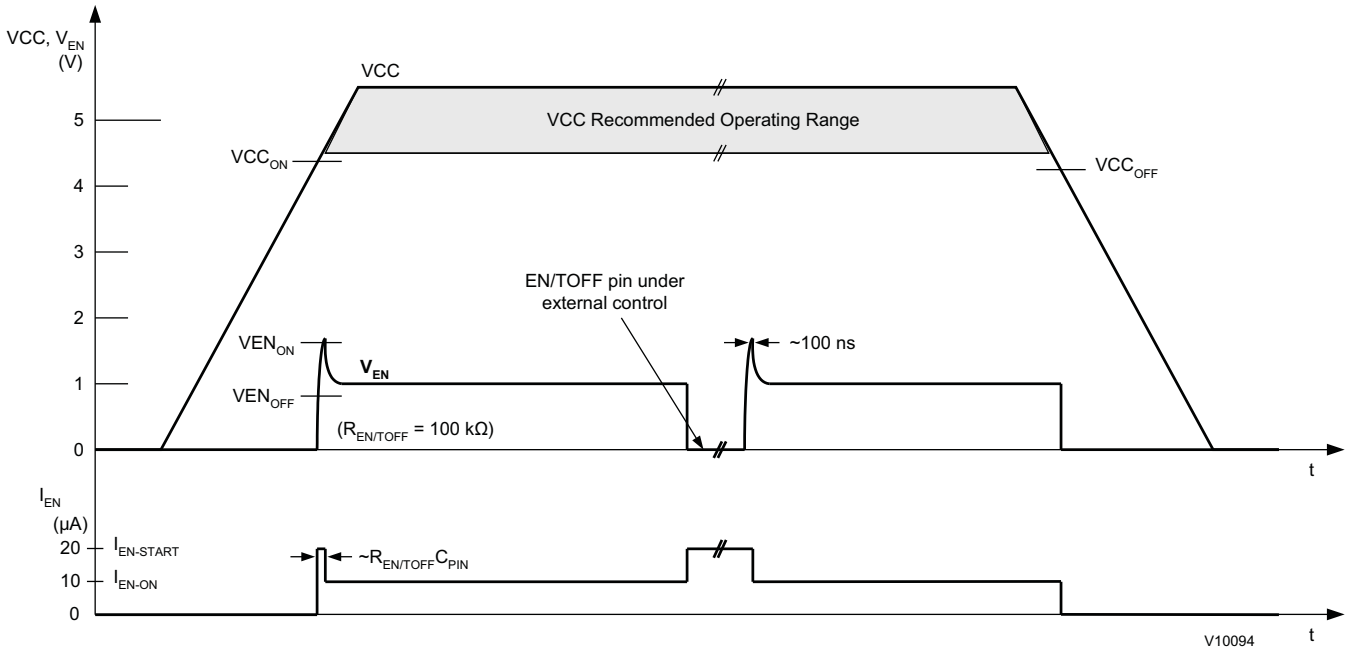


Figure 17. Behavior of I_{EN} and V_{EN} as VCC Varies ($R_{EN/TOFF}$ = 100 kΩ)

The UCC24610 SR controller determines the conduction time of the SR-MOSFET by comparing the MOSFET's drain-to-source voltage against a turn-on threshold and a turn-off threshold. The GATE output is driven High when V_{DS} of the MOSFET exceeds $V_{TH(on)}$ and is driven Low when V_{DS} decreases below $V_{TH(off)}$ as illustrated in Figure 18.

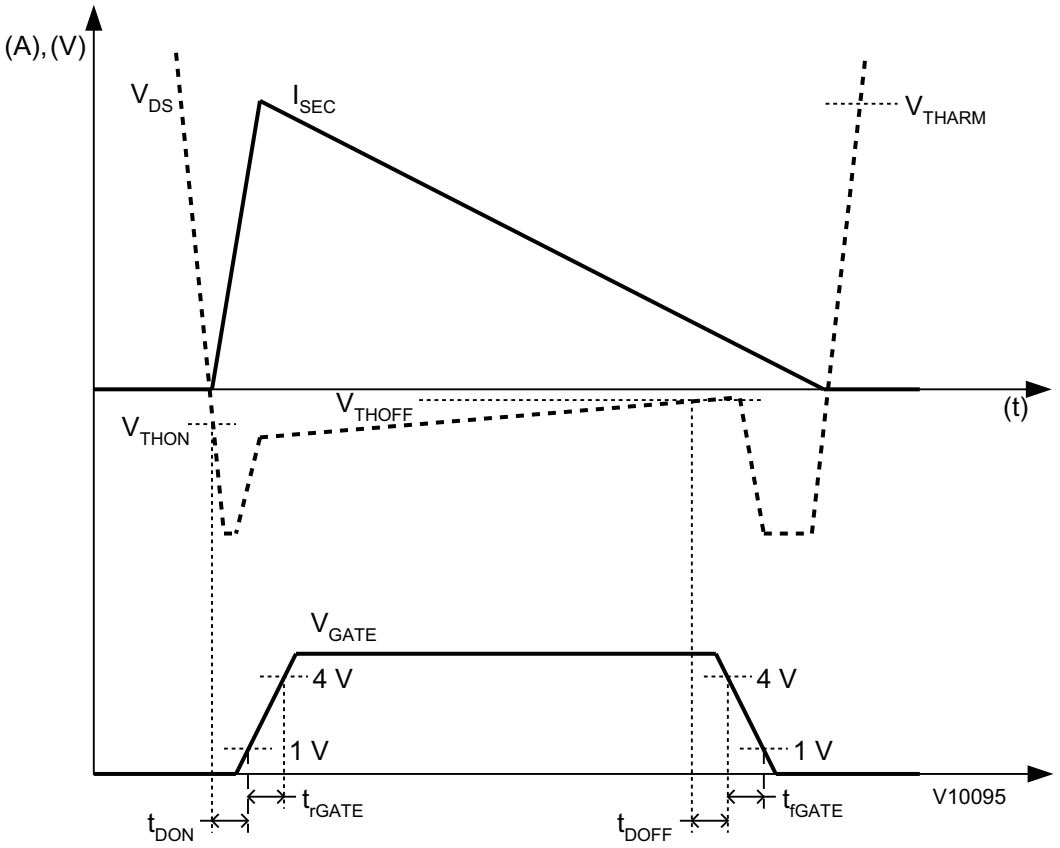


Figure 18. GATE Output With Respect to V_{DS}

Note that because of finite propagation and rise times, the body diode of the SR-MOSFET may conduct briefly after $V_{TH(on)}$ has been exceeded. Also, the body-diode conducts the residual secondary current after $V_{TH(off)}$ has been crossed. A waveform similar to that of V_{DS} depicted in Figure 18 can be observed during SR operation in a simple flyback circuit.

However, actual in-circuit waveforms are rarely as clean as shown in Figure 18. Instead, parasitic inductances and capacitances set up resonant ringing at various inflection points in the waveforms. The UCC24610 has control timing and programming options which helps avoid interference from such ringing with proper operation. Figure 19 shows more realistic waveforms and the internal control timing which accommodates them. The waveforms affecting the SR-MOSFET in a typical flyback circuit are shown.

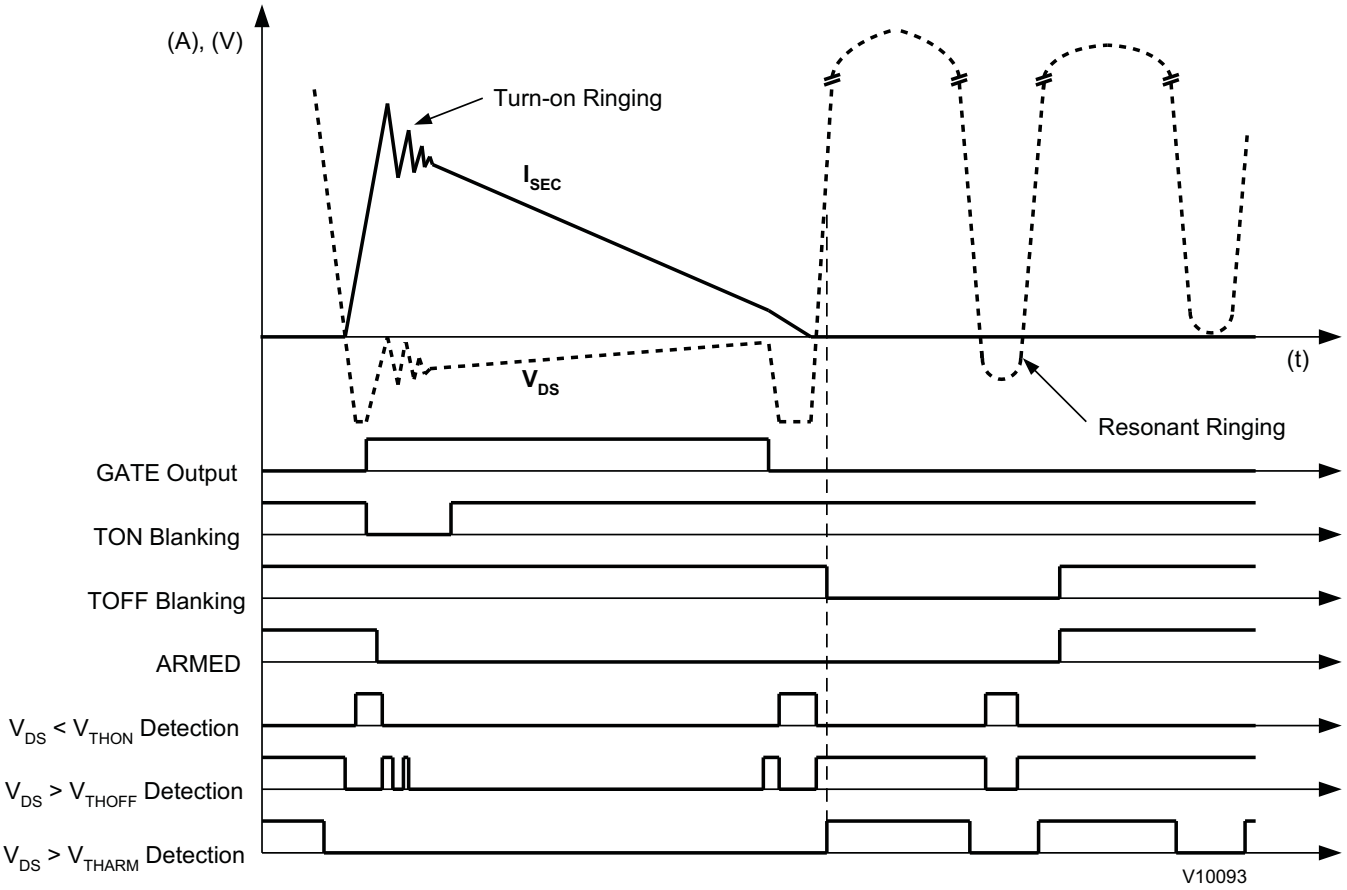


Figure 19. Internal Signal Timing With Respect to Realistic DCM Waveforms

Minimum on-time TON is programmed with a resistor from TON, (pin 3) to GND to blank the response of the turn-off detection circuit to prevent GATE from being turned-off from spurious crossings of $V_{TH(off)}$ due to noise and ringing. TON is triggered by the GATE turning on. Refer to the TON programming section below for details.

Minimum off-time T_{OFF} is programmed with a resistor from pin 2 to GND to blank the response of the turn-on detection circuit to prevent GATE from being turned-on again from spurious crossings of $V_{TH(on)}$ due to excessive C_{OSS} resonant ringing. TOFF is triggered by V_{DS} crossing V_{THARM} after the GATE turns off. Refer to the TOFF programming section below for details.

The GATE output may only turn on when the controller has been “armed” for the switching cycle. The controller is armed for each successive SR cycle only after TOFF expires. Note that in high-frequency applications, an excessively long TOFF may interfere with timely turn-on of GATE in the next switching cycle. GATE turn on will be delayed if TOFF from the previous cycle has not yet expired.

Light-Load Operation

During normal operation, the synchronous rectifier conduction time is longer than the programmed minimum on-time. If load current decreases enough that the SR conduction time becomes shorter than the programmed minimum on-time, a light-load condition is detected. The light-load latch is set and the next GATE output pulse is blanked, so only the body diode of the controlled MOSFET conducts. This comparison between SR conduction time and minimum on time occurs every switching cycle, regardless of whether the GATE output pulse is enabled or blanked. When load current increases enough that the body-diode conduction time becomes longer than the programmed minimum on time, the light-load latch is cleared and the next GATE output pulse is enabled and the controlled MOSFET resumes SR operation.

Figure 20 depicts the progression into Light-Load Mode for a DCM flyback application as the load decreases, while Figure 21 depicts the reverse progression back to Run Mode.

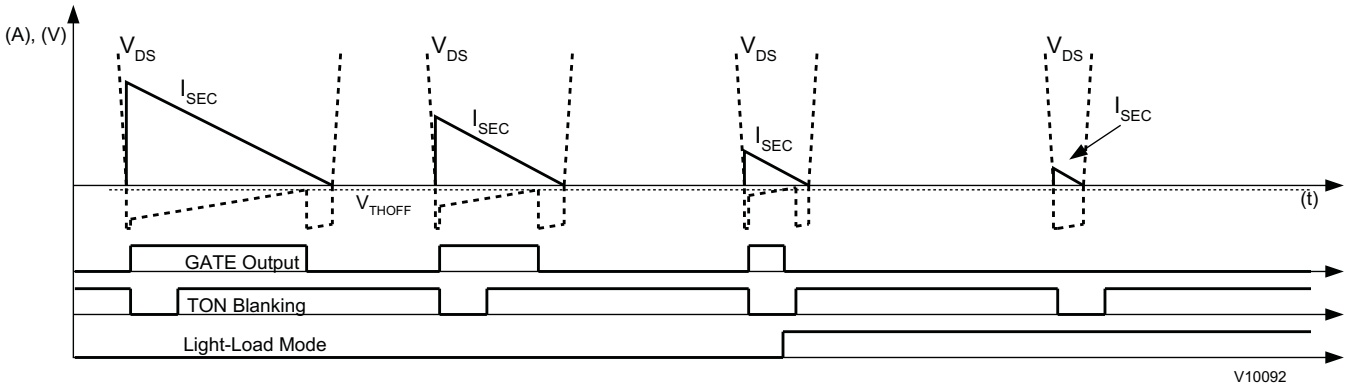


Figure 20. Decreasing Load Current Progression Leads to Light-Load-Mode Operation

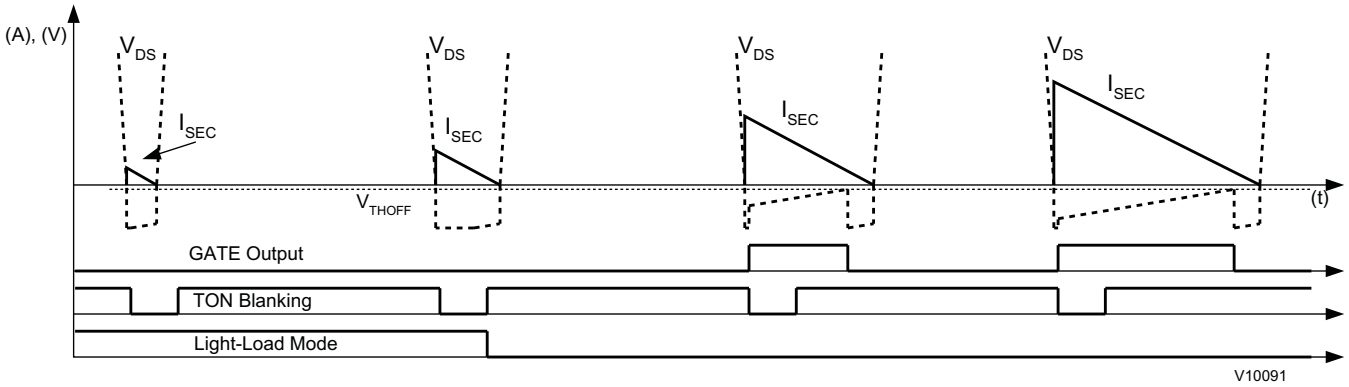


Figure 21. Increasing Load Current Progression Returns to Run-Mode Operation.

Application Considerations

VD and VS Detection

VD and VS are differential inputs used to sense the voltage across the SR-MOSFET to determine when to turn on and off the GATE output. When the GATE is off, the controller will not drive the GATE on until VD has exceeded 1.5 V at least once and TOFF has expired. Once these two conditions are met, the controller is *armed* to allow the GATE to turn on the next time the drain voltage falls 150 mV below the source voltage (VD - VS = -150 mV). While the GATE is off, the SR-MOSFET may be blocking reverse current, or forward current may be building up in the MOSFET body diode. Normally this body-diode current would generate about 700 mV forward voltage drop (-700 mV_{DS}), but when -150 mV is detected the GATE is turned on to enhance the MOSFET into a synchronous rectifier. The GATE stays on for at least the minimum on time TON or longer until the SR-MOSFET current diminishes to near zero. When the current reduces sufficiently such that the V_{DS} voltage drop is only -5 mV, the GATE output is turned off. (It can be seen that the MOSFET $R_{DS(on)}$ determines the current level at which the GATE is turned off, which then further factors into determining the Light-Load Mode inception point.) At the same time, the controller is *disarmed* to prevent spurious GATE output. Because the MOSFET current is not yet zero at GATE turn off, the V_{DS} will briefly increase back up to the body-diode drop, however the additional power loss is very small. The *disarmed* state of the controller prevents repeated turn on of the GATE (even though V_{DS} < -150 mV again). Once the current does decrease to zero, the drain voltage climbs past the 1.5-V threshold, at which point the minimum off-time interval TOFF is triggered. Once V_{DS} has exceeded 1.5 V and TOFF has expired, the GATE circuit is *re-armed* to respond to the next turn-on condition.

Because the VD and VS inputs are connected across the SR-MOSFET body diode by way of its package leads, the high secondary-side dI/dt through the lead inductances can impress excessive negative voltage on the VD pin. This negative voltage can disrupt normal controller operation and prevent the device from switching. This problem can be avoided by limiting the current drawn out of the VD pin to less than 100 mA. A resistor placed in series between VD and the SR-MOSFET drain can be sized to provide the proper current limiting.

This resistor value is calculated by:

$$R_{VD} \geq \frac{\left(L_{PKG} \frac{dI_{SEC}}{dt} - 0.3\,V \right)}{0.1A} \tag{1}$$

where L_{PKG} is the total package inductance between the drain and source pads of the SR-MOSFET when mounted on the PCB, and dI_{SEC}/dt is the rate of rise of the secondary current after the primary-side switch turns off. Include any stray trace inductance if the device GND pin is not connected directly to the SR-MOSFET source pad.

The bias current of the VD pin through R_{VD} (if any) generates a small offset voltage which can cause an apparent shift in the SR-MOSFET turn-off threshold, leading to earlier turn off than desired, depending on the value of R_{VD}. To counter this offset voltage, a resistor of equal value can be placed in series with the VS pin to balance the VD-VS comparator inputs ($R_{VS} = R_{VD}$).

Larger MOSFET packages such as TO-220 and TO-247 generally have significant internal inductances (on the order of 10 nH ~ 20 nH), and are used in higher-power applications where dI/dt can be quite high. On the other hand, low-power applications using smaller packages such as QFN style and even DPAK™ or equivalent MOSFETs can have a sufficiently low L x dI/dt product such that R_{VD} and R_{VS} may not be necessary. Refer to the MOSFET datasheet or consult with the manufacturer to determine the total inductance for the specific MOSFET being considered for a synchronous-rectifier application.

Enabling and TOFF Programming

The controller must be out of UVLO Mode, or the internal current source on EN/TOFF pin is shut off and the pin is pulled low with an internal 10-kΩ resistor. Before the device is in the Enabled state, the current source on EN/TOFF delivers 20 μA. Prudent design practice indicates that a minimum $R_{EN/TOFF}$ value of 93 kΩ is necessary to ensure the pin voltage exceeds the disable threshold. After being Enabled, the Enabled state is latched and the source current reduces to 10 μA. This current level establishes the voltage which determines the TOFF time, as programmed below.

Once both the VCC and EN/TOFF conditions are met to enable the device, an internal power-up sequence ensures that the controller starts the SR-MOSFET synchronously with the system conduction conditions. This avoids turn-on of the SR-MOSFET into an inappropriate system state. After a ~25-μs delay to allow internal references to stabilize, SR operation commences in Light-Load Mode and the load condition is monitored at the first complete switching cycle after the delay to determine the next operating mode.

Because V_{DS} of the SR-MOSFET may ring above 1.5 V and back below -150 mV one or more times (due to circuit parasitic elements), TOFF time should be programmed to block GATE re-arming for the duration of this ringing. In a system, the duration of this ringing may be unknown until actual prototypes are operational and observable, so a longer TOFF time may be initially programmed and the final value adjusted after system evaluation and optimization.

Nominal TOFF off time is programmed by the following formula, where TOFF is in μs and $R_{EN/TOFF}$ is in MΩ:

$$TOFF(\mu s) = \left(11(\mu s) - 39\left(\frac{\mu s}{M\Omega}\right) R_{EN/TOFF}(M\Omega) \right) + 0.65(\mu s)(min) \quad (2)$$

valid for:

$$0.1 \le R_{EN/TOFF}(M\Omega) \le 0.282 \quad (3)$$

Conversely,

$$R_{EN/TOFF}(M\Omega) = \frac{\left(11(\mu s) + 0.65(\mu s)(min) - TOFF(\mu s)\right)}{39\left(\frac{\mu s}{M\Omega}\right)} \quad (4)$$

valid for:

$$0.65 \le TOFF(\mu s) \le 7.75 \quad (5)$$

For any $R_{EN/TOFF}$ > 282 kΩ, TOFF = 0.65 μs.

For any 70 kΩ < $R_{EN/TOFF}$ < 80 kΩ, V_{EN} toggles rapidly between 1.4 V and 0.8 V and the device remains disabled. In this situation, average I_{CC} is approximately half of the normal Run-Mode current, $I_{CC(on)}$.

For any $R_{EN/TOFF}$ < 70 kΩ, VEN is < 1.4 V and the device is disabled, operating in Sleep Mode.

TON Programming

The voltage on this pin is internally regulated to 2 V, and an external resistor to GND sets a current which programs the minimum on time TON. If a noise-filter capacitor is deemed to be necessary on this pin, do not exceed 100 pF to avoid instability of the 2-V regulator.

Because V_{DS} of the SR-MOSFET may ring above -5 mV one or more times immediately after turn on (due to circuit parasitic elements) TON time should be programmed to block GATE turn off for the duration of this spurious ringing. In a system, the duration of this ringing may be unknown until actual prototypes are operational and observable, so a longer TON time may be initially programmed and the final value adjusted after system evaluation and optimization.

Nominal TON minimum on time is programmed by the following formula, where TON is in µs and R_{TON} is in MΩ:

$$TON(\mu s) = 15\left(\frac{\mu s}{M\Omega}\right) R_{TON}(M\Omega) \tag{6}$$

Valid for:

$$0.010 \le R_{TON}(M\Omega) \le 0.301 \tag{7}$$

Conversely,

$$R_{TON}(M\Omega) = \frac{TON(\mu s)}{15\left(\frac{\mu s}{M\Omega}\right)} \tag{8}$$

Valid for:

$$0.15 \le TON(\mu s) \le 4.5 \tag{9}$$

For resistance values of R_{TON} outside of the valid range given above, the device may enter a Fault-Protection Mode as detailed below.

GATE Drive and R_{GATE} Considerations

The GATE output driver is capable of sourcing >1-A peak current into the SR-MOSFET gate, and sinking >2 A out of it. Standard low-inductance, low-loop-area design techniques should be employed to minimize stray inductance which slows the MOSFET turn on and increases gate-drive ringing.

A series resistance R_{GATE} from the GATE output to the MOSFET gate is used to damp this ringing, and its value is chosen based on the standard critical damping formula for a series-LCR resonant tank.

$$R_{GATE} \geq 2\sqrt{\frac{L_g}{C_{iss}}} - r_g \tag{10}$$

where L_g is the total series gate-loop inductance, C_{iss} is the total effective input capacitance of the MOSFET, and r_g is the internal gate resistance of the MOSFET.

Please note that the total series resistance in the gate-drive path may also limit the peak GATE currents obtainable below the rated capabilities of the device's GATE output driver stage.

VCC Range and Bypassing Considerations

With a normal operating range of 4.5 V to 5.5 V, the device is well suited for 5-V nominal output applications and can easily accommodate +/-10% transient VCC excursions due to system line and load disturbances. When the average VCC voltage approaches the $V_{CC(off)}$ threshold (UVLO), system ripple and noise on VCC may cross that threshold and shut down the controller unless adequate decoupling is provided from VCC to GND at the controller pins.

High peak gate-drive currents during the GATE turn-on transition also require sufficient local capacitive bypassing of the VCC pin to GND. For smaller SR-MOSFETs a minimum value of 0.1 μF may be sufficient, but larger MOSFETs may require additional bypass capacitance to avoid excess ripple on the VCC voltage.

Suggested VCC bypass capacitance is 0.1 μF for each 2.2 nF of C_{iss}.

SYNC Input Considerations

In applications where the synchronous rectifier is used in Continuous Conduction Mode (CCM) such as CCM-Flyback and LLC converters, it is imperative that the SR-MOSFET be turned off as soon as the primary-side switch turns on, to prevent reverse conduction of the SR-MOSFET. In these applications, a Y-type isolating capacitor C_{SYNC} can be used to convey a primary-side signal to the SR controller by coupling a negative-going trigger voltage into the SYNC pin. Alternatively, an isolating pulse transformer may be used in situations where a coupling capacitor is not practicable. When the SYNC voltage falls 2 V below VCC (the SYNC detection threshold V_{THSYNC}), the GATE output is immediately turned off, regardless of the state of the TON timer. An internal 2-kΩ pull-up resistance (r_{SYNC}) provides current to recharge the SYNC coupling capacitor. In the event that the SYNC input voltage is continuously held below V_{THSYNC}, the GATE output is driven low for the same duration.

The SYNC input has a maximum pulse current rating of ±100 mA, and a high-reliability design should reduce the peak current further. This also reduces noise and signal losses in the system. A series resistor helps limit the pulse current by reducing the effective dV/dt across C_{SYNC}. Figure 22 illustrates a simple implementation of the SYNC signal derived from the falling drain-source voltage of the primary-side MOSFET. In this example, a synchronous-rectifier MOSFET is used in place of the free-wheeling diode in a single-transistor forward-mode application. Note that primary-to-secondary common-mode capacitance CCM forms the return path for the SYNC current.

Nominally, only -1 mA is required to develop -2 V across the internal 2-kΩ resistance and trigger the SYNC function. This current is generated by a rapidly changing voltage across the SYNC coupling capacitor C_{SYNC}. But variations of this resistor, of C_{SYNC}, and of the dV/dt across C_{SYNC} require that worst-case tolerances be taken into account when determining the minimum value of C_{SYNC}. In addition, V_{SYNC} must exceed the V_{THSYNC} threshold for a minimum duration of 20 ns to ensure that the internal controller logic has reliably triggered.

Although the TON minimum on-time gate-drive function is overridden by the SYNC signal, the timer continues to function otherwise. Light-Load Mode is entered if the proper conditions are met, as usual. The TOFF timer is triggered when the SR-MOSFET V_{DS} exceeds 1.5 V, as usual.

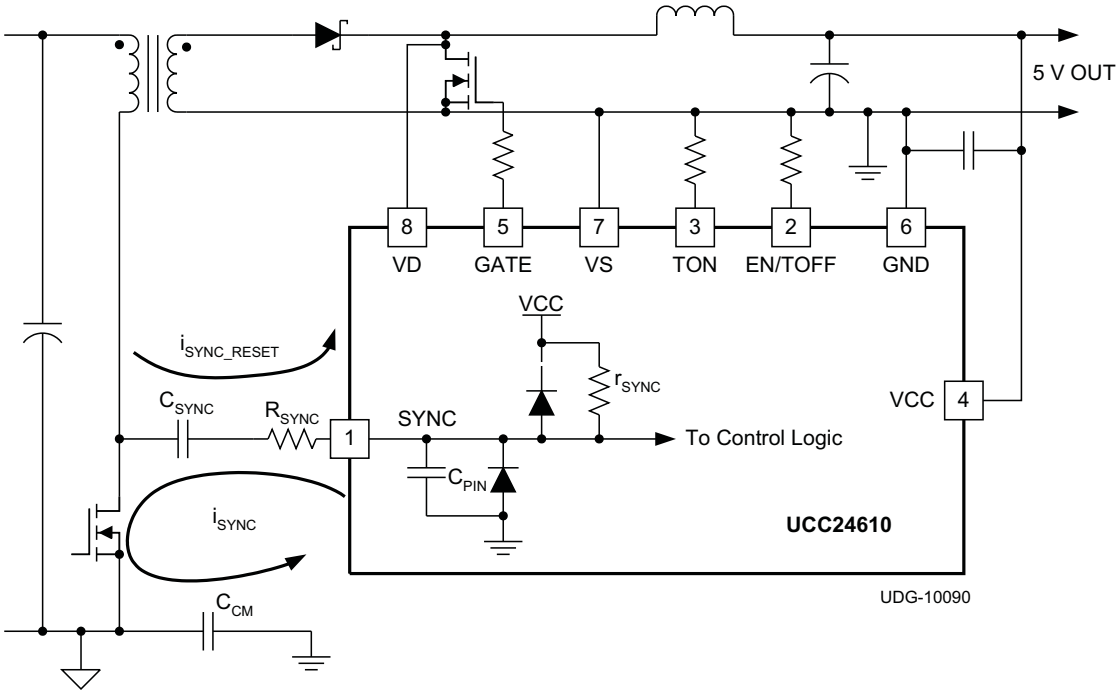


Figure 22. Driving the SYNC Input from the Primary-Side MOSFET Drain

C_{SYNC} is the synchronization signal coupling capacitor, rated to cross the primary-to-secondary isolation boundary. It is used to couple a negative-going voltage into the UCC24610 SYNC input (pin 1) to turn off the GATE output to the SR-MOSFET when the primary-side MOSFET is turned on.

R_{SYNC} is an optional external current-limiting resistor used to reduce the peak current into the SYNC input. It also serves to reduce overall power loss, and reduce the common-mode noise current.

C_{CM} is the main common-mode capacitance between the primary and the secondary sides of the system. This is usually a discrete component, whose value ranges from 100 pF ~ 2200 pF. Aside from any EMI-control purposes, it also serves as the return path for the SYNC signal charging and discharging current pulses across the isolation boundary.

Within the UCC24610 controller device is a 2-kΩ pull-up resistor (r_{SYNC}) to VCC. To trigger the SYNC function, a negative-going signal must pull the SYNC input below the V_{THSYNC} threshold (nominally 2 V below VCC) for a minimum duration of 20 ns. This requires a minimum 1-mA current to achieve, but prudent design will target a higher current to allow for parameter variations.

Internal clamp diodes to VCC and GND also form parts of the charging and discharging current paths of the SYNC signal. Finally, C_{PIN} comprises stray internal and external pin and pad capacitances on the SYNC input, and is modeled as ~10 pF to GND. Although C_{PIN} is physically unavoidable, it is wise to minimize any external stray capacitance to keep its effect of additional delay on the SYNC function to a minimum.

1. Determine the Minimum Change

Determine the minimum change in voltage $\Delta V_{SYNC\text{-}pri}$ expected from the SYNC signal source. In this example, the primary-side MOSFET drain-to-source voltage V_{DS_PRI} is the signal source, and its minimum change is $V_{BULK(min)}$ at low input line.

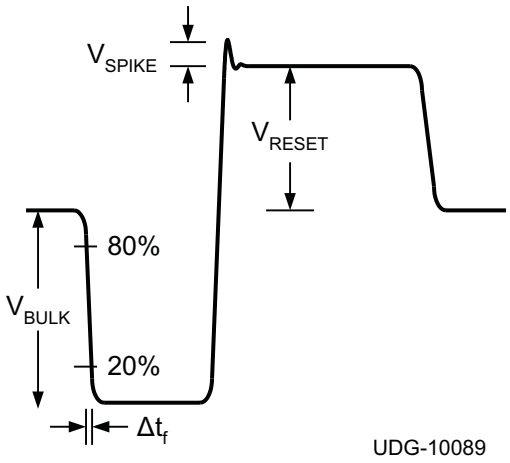


Figure 23. Primary MOSFET Drain Voltage

$\Delta V_{DS\_PRI} = V_{BULK}$ at low-line. Δt_f = fall time for ΔV_{DS_PRI} between the 80% and 20% points.

$V_{SYNC\text{-}pri} = \Delta V_{DS\_PRI}$

To allow for parameter and environmental variations, set the minimum peak SYNC current to be 2 mA. With 2 mA peak flowing through the internal 2-kΩ resistor, the SYNC voltage falls to 4 V below VCC. The maximum value for current limiting resistor R_{SYNC} is determined by:

$$R_{SYNC} \le \frac{\Delta V_{SYNC-pri}}{i_{SYNC}(min)} - r_{SYNC} \tag{11}$$

so in this case,

$$R_{SYNC} \le \frac{V_{BULK}(min)}{2mA} - 2k\Omega \tag{12}$$

2. After the ΔV_{DS_PRI} Transition

After the ΔV_{DS_PRI} transition, the SYNC signal will begin to reset back to VCC by charging exponentially. This allows the value of the SYNC coupling capacitor C_{SYNC} to be determined by:

$$C_{SYNC} = \frac{1.5 \times t_{MIN}}{R_{SYNC} + r_{SYNC}} \tag{13}$$

The value of C_{SYNC} is chosen to ensure that the SYNC signal stays below the SYNC threshold for at least 20 ns. Choose the minimum dwell time t_{MIN} to be 40 ns to allow for parametric variations, so in this case:

$$C_{SYNC} = \frac{1.5 \times 40\,ns}{R_{SYNC} + 2k\Omega} \tag{14}$$

3. The value of C_{CM}

The value of C_{CM} should be much higher than that of C_{SYNC}. If necessary, increase the value of C_{CM} to ensure that C_{CM} >> C_{SYNC}; do not decrease C_{SYNC}.

4. Conservative Power-Loss Estimates

Conservative power-loss estimates for the internal and external SYNC resistances are:

$$P_{r_{SYNC}} \le \left[\frac{(VCC + 0.7\,V)^2}{r_{SYNC}}\right] \times \left[\ln\left(\frac{\Delta V_{SYNC-pri-max}}{\Delta V_{SYNC-pri-min}}\right) + 1\right] \times \left[(R_{SYNC} + r_{SYNC}) \times C_{SYNC} \times f_{SW}\right] \tag{15}$$

and

$$P_{R_{SYNC}} \le 2 \times \left[\frac{1}{2} \times C_{SYNC} \times (V_{BULK} + V_{RESET} + V_{SPIKE})^2 \times f_{SW}\right] \tag{16}$$

where f_{SW} is the converter switching frequency. These calculations can be used to predict the maximum thermal impact of the SYNC current on the device junction temperature and to determine the external SYNC resistor power rating. Actual SYNC-related losses generally are lower than these calculations predict and observations of actual circuit operation should be used to determine true losses if more accuracy is required.

5. The Device Internal SYNC-to-GATE Delay Time

The device internal SYNC-to-GATE delay time t_{SDLY} is a measure of how quickly the GATE output will turn off after the SYNC signal has crossed the V_{THSYNC} threshold. However, stray pin capacitance C_{PIN} introduces an additional delay to the SYNC function by slowing the SYNC voltage falling 2 V below VCC. If C_{PIN} is small, this delay is relatively short and the SYNC current can be approximated as a constant current, allowing this calculation to simplify to a simple linear equation given by:

$$t_{PIN\_DLY} = \frac{2\,V \times C_{PIN}}{i_{SYNC}} \tag{17}$$

Also, additional delay comes from the finite dV/dt of the signal source, in this case V_{DS_PRI}, due to the finite transition time from V_{BULK} level to 0 V. This delay can be approximated by:

$$t_{dV\_DLY} = \frac{\Delta t_f \times R_{SYNC}}{R_{SYNC} + r_{SYNC}} \tag{18}$$

These delay times should be added to the internal SYNC-to-GATE delay (specified in the datasheet) to determine the total delay time expected between the falling of the primary-side MOSFET drain voltage and the turn off of the SR-FET gate drive.

$$t_{OFF\_DLY} = t_{SDLY} + t_{PIN\_DLY} + t_{dV\_DLY} \tag{19}$$

6. The C_{SYNC} Capacitor Resets

The C_{SYNC} capacitor resets during the off-time of the primary-side MOSFET, while the SR-FET is conducting. The reset current i_{SYNC_RESET} is similar to i_{SYNC}. However, this reset current flows through the internal diode between SYNC and VCC pins of the device.

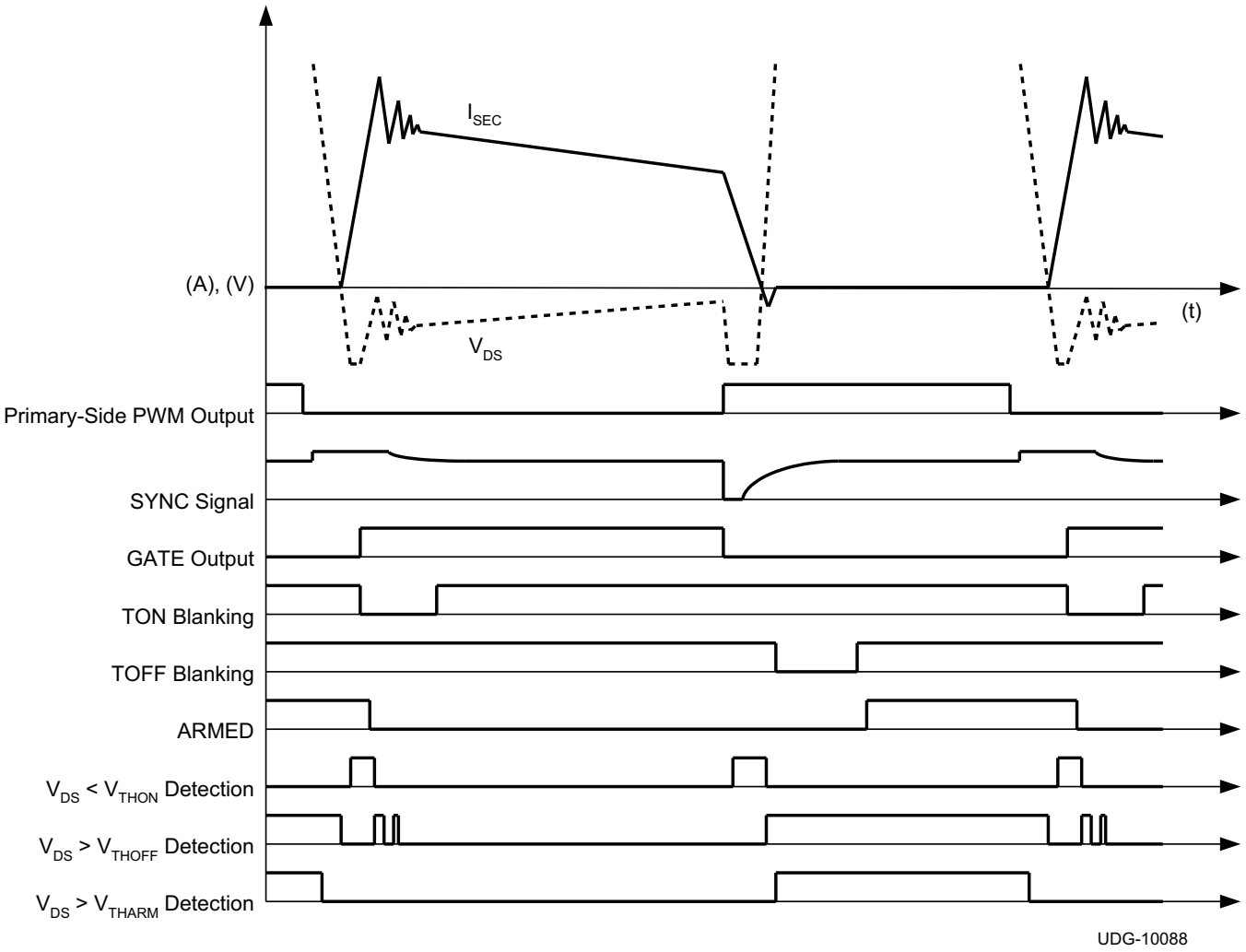


Figure 24. External and Internal Signal Timing Relationships with Respect to Realistic CCM Waveforms

Single-Fault Self-Protection Features

If R_{TON} is less than 8.7 kΩ, the device may detect excess current and interpret this as a short-cir cuit and disable the GATE output.

If R_{TON} is greater than 301 kΩ, the device may detect insufficient current and interpret this as an open-circuit and disable the GATE output, to avoid indefinite on-time.

Noise pick-up on excessive trace length may destabilize the internal 2-V source causing either insufficient or excess current to R_{TON} and triggering premature GATE shut off. This could cause GATE output to be less than TON and lead to Light-Load Mode even at heavy loads. Minimize R_{TON} trace lengths.

If $R_{EN/TOFF}$ is less than 93 kΩ, the device may detect insufficient voltage for Enable threshold and disable the GATE output.

If $R_{EN/TOFF}$ is greater than 284 kΩ, the device will internally clamp the programming voltage to deliver a minimum T_{OFF} of ~0.65 µs, regardless of $R_{EN/TOFF}$ value.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
HPA01055DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC24610D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC24610DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC24610DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC24610DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

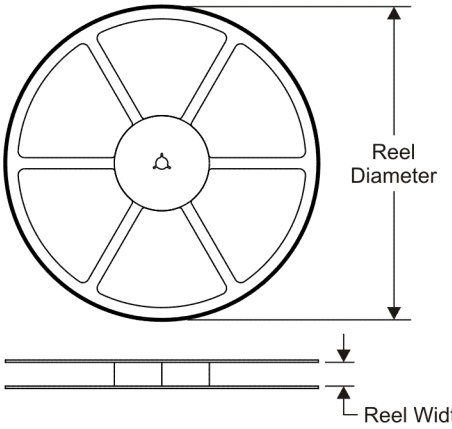
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

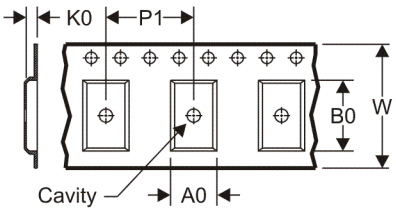
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

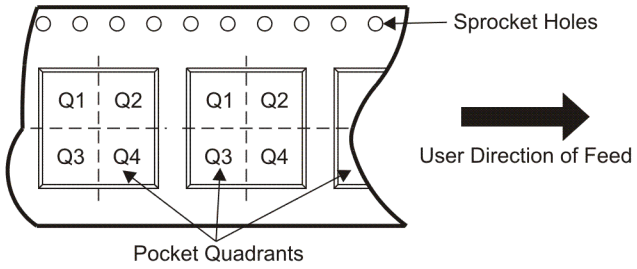


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

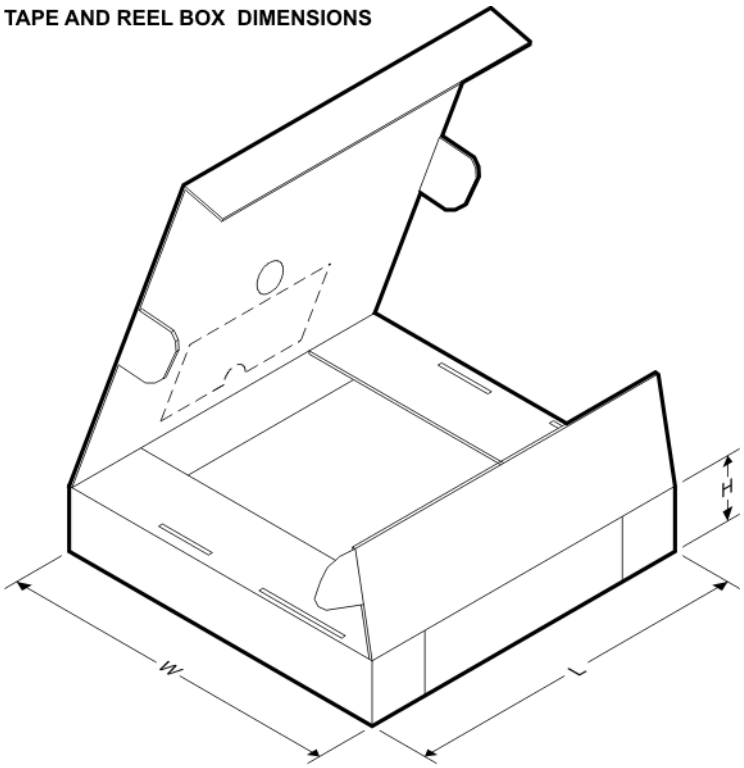
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC24610DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC24610DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
UCC24610DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

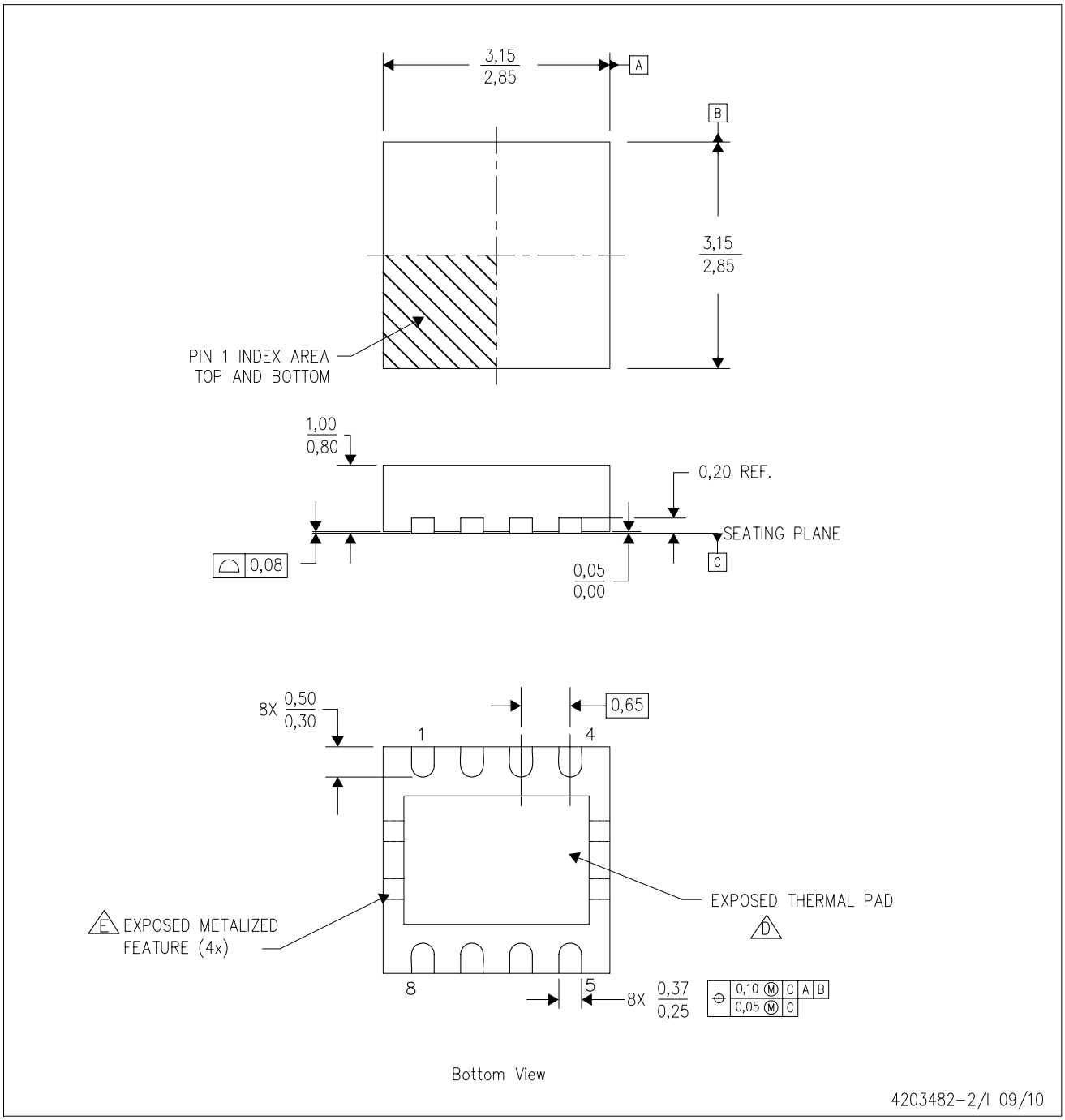
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC24610DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC24610DRBR	SON	DRB	8	3000	346.0	346.0	29.0
UCC24610DRBT	SON	DRB	8	250	190.5	212.7	31.8

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

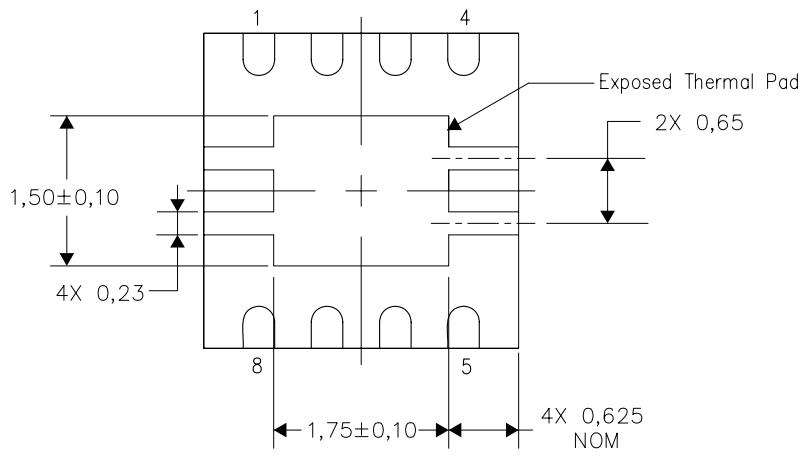
DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



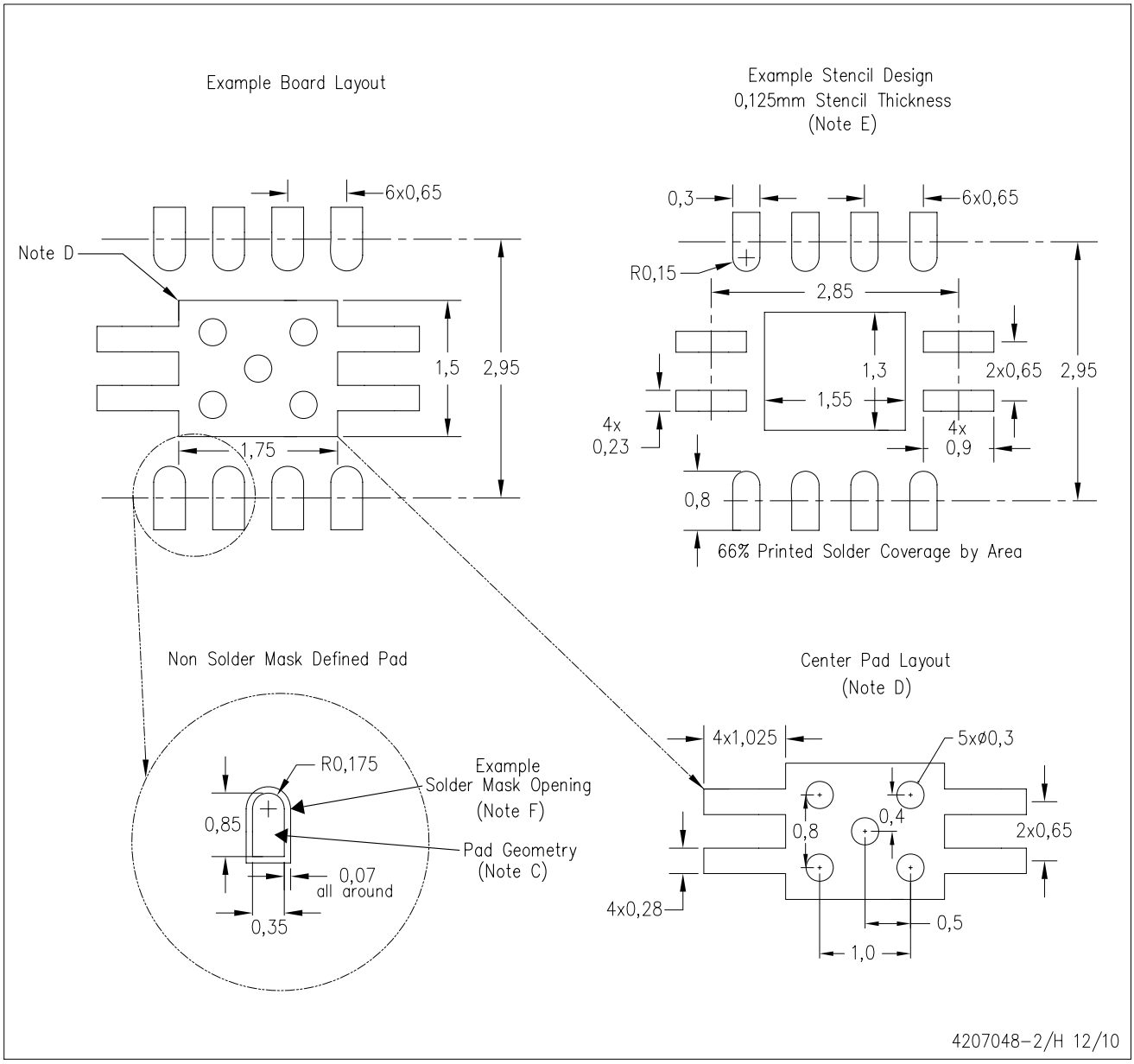
Bottom View

Exposed Thermal Pad Dimensions

4206340–2/L 12/10

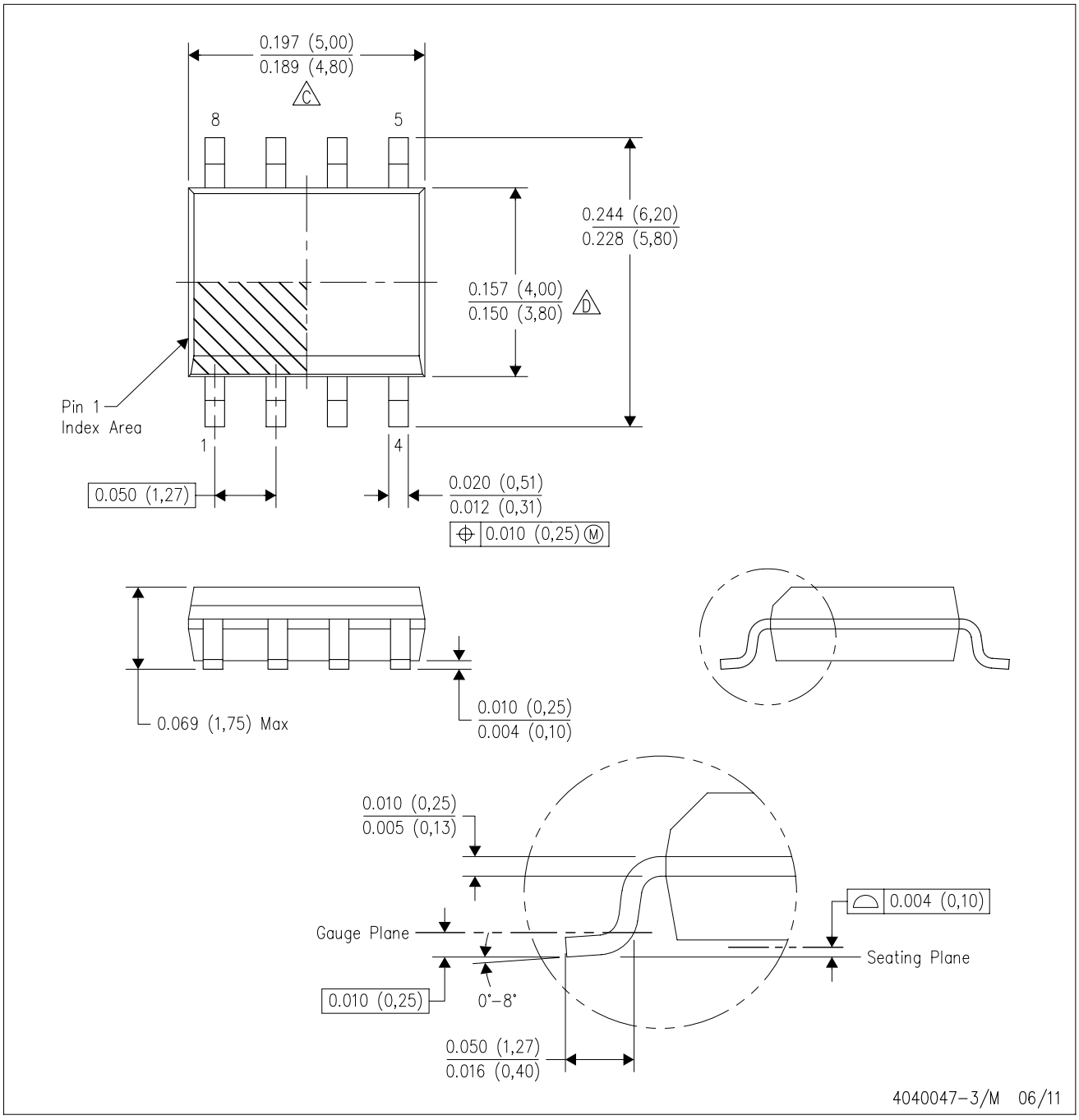
NOTE: A. All linear dimensions are in millimeters

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



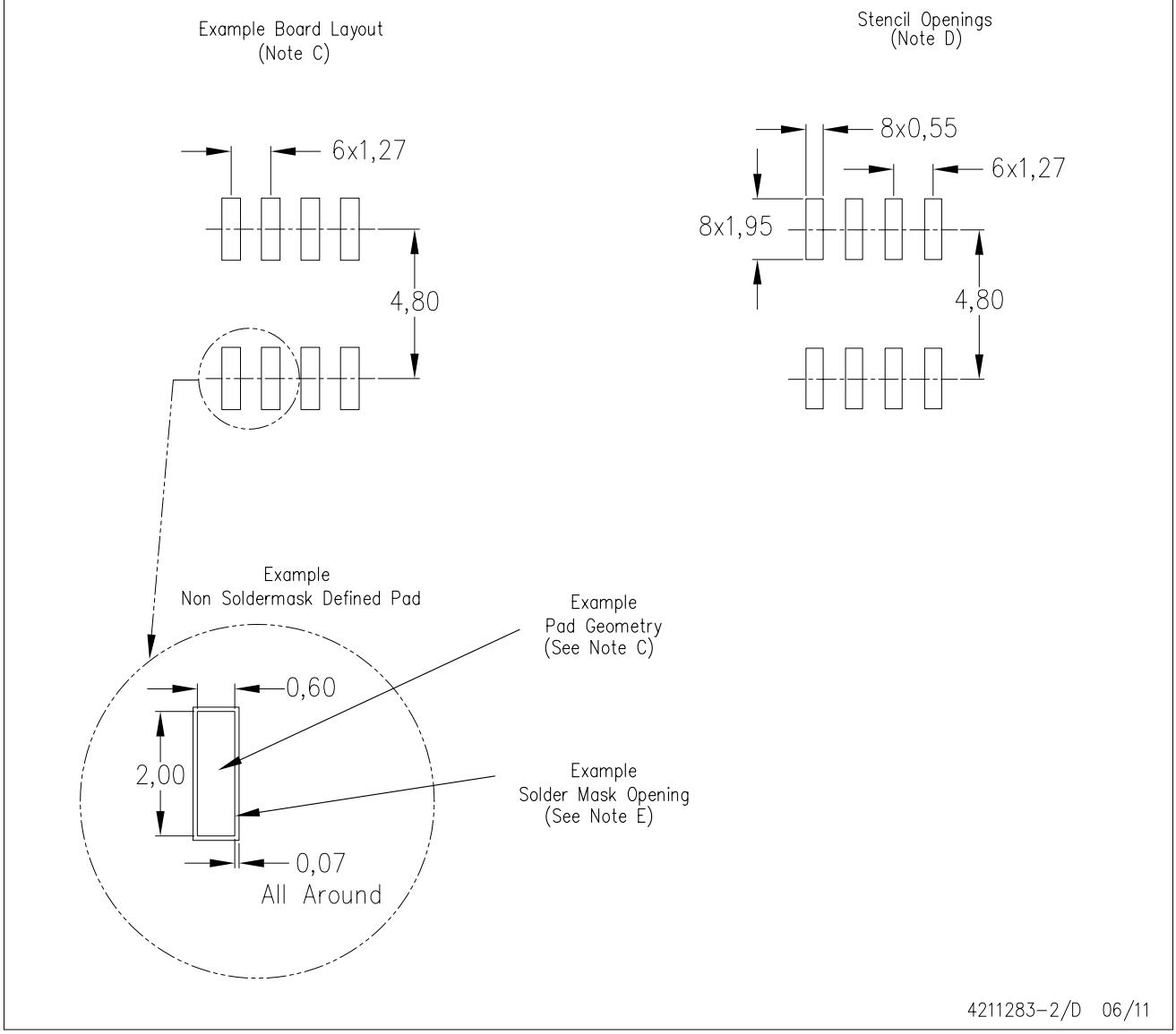
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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